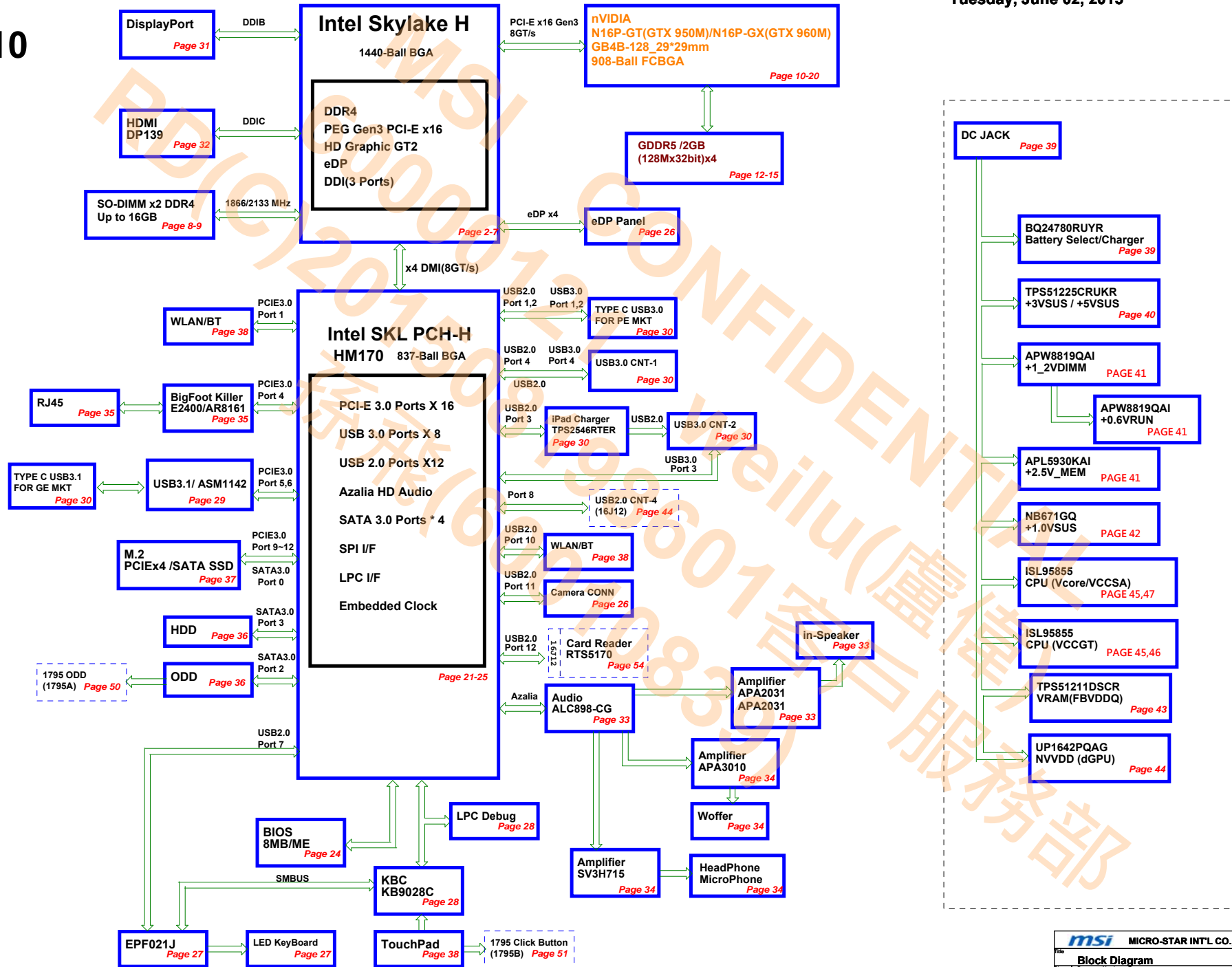


Ver:10

Tuesday, June 02, 2015

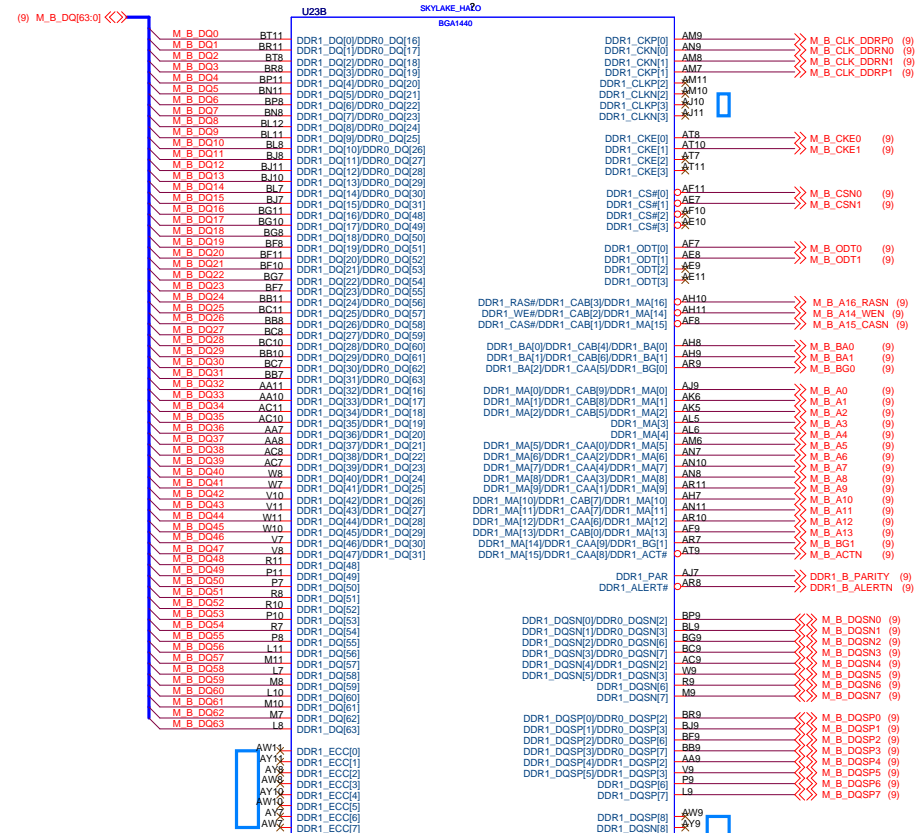








## DDR Channel B



DDR CHANNEL B

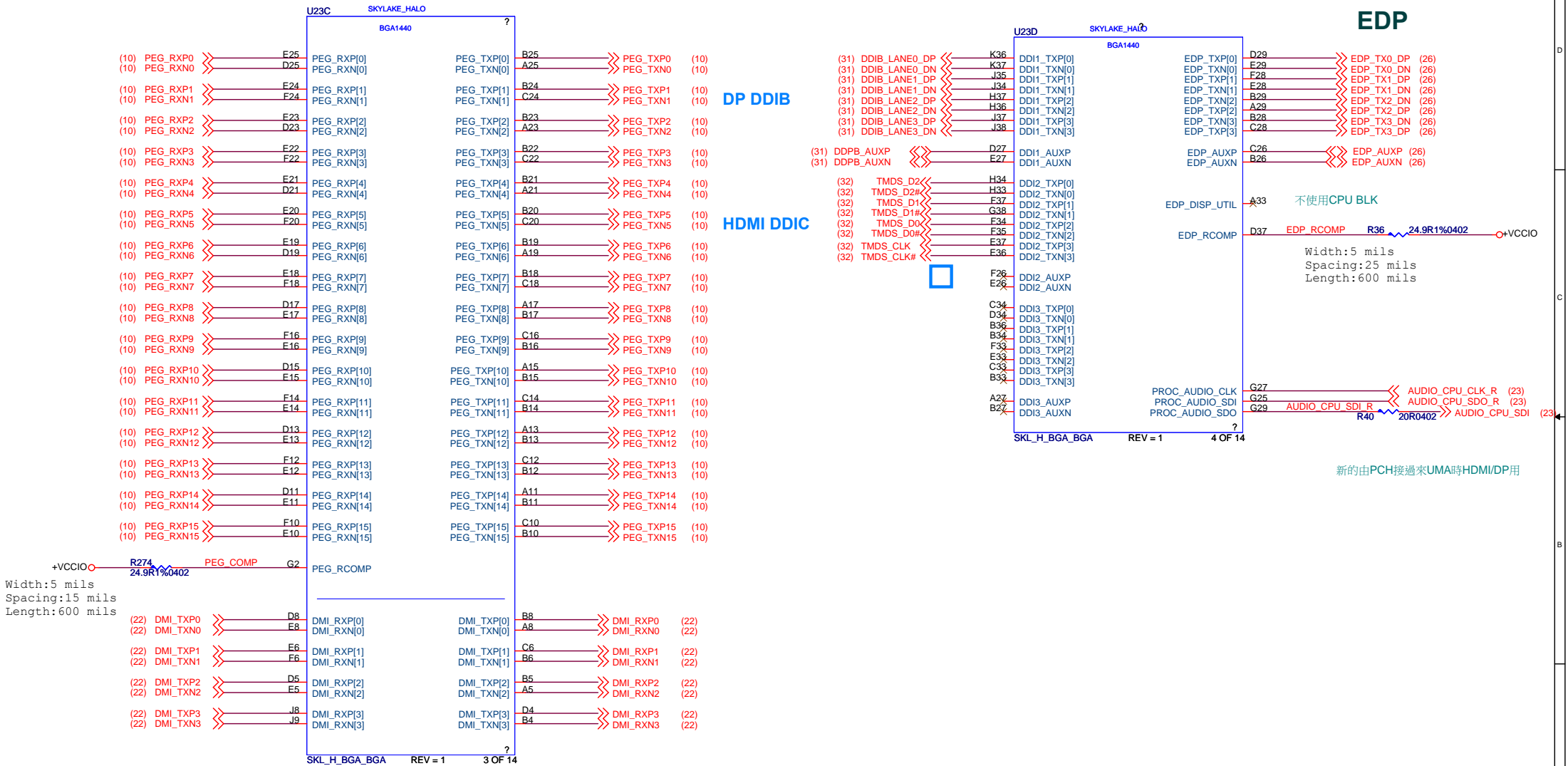
SKL\_H\_BGA\_BGA

REV =

2 OF 14

 DG Page 157





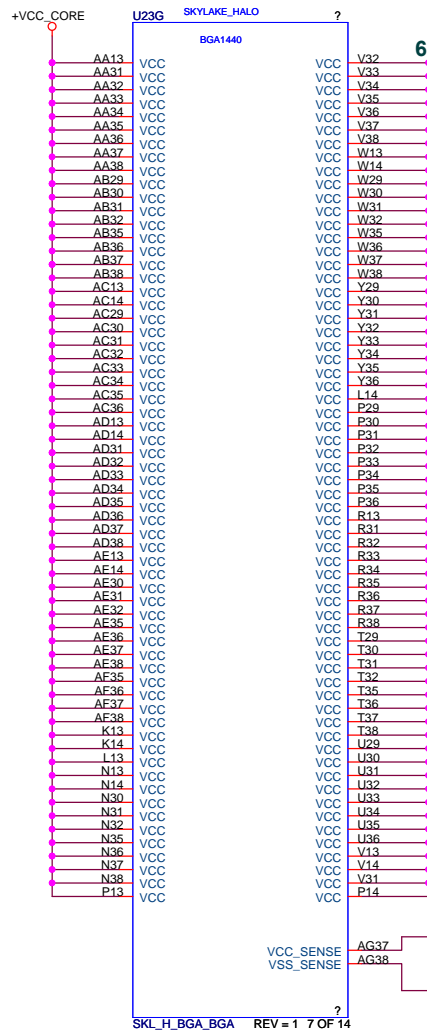
Width:5 mils  
Spacing:15 mils  
Length:600 mils

不使用CPU BLK  
Width:5 mils  
Spacing:25 mils  
Length:600 mils

新的由PCH接過來UMA時HDMI/DP用

msi MICRO-STAR INT'L CO.,LTD.		
Title		
Skylake(DMI/Display)		
Size	Document Number	Rev
B	MS-16J5	10
Date:	Tuesday, June 02, 2015	Sheet 4 of 55

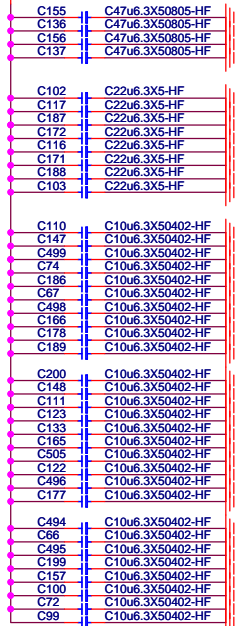




68A

+VCC\_CORE

+VCC\_CORE



少63顆0201 1UF電容

10uF 換幾顆1uF 靠近BALL C11-105A312-M09(X6S)

10uF 更改FOOTPRINT

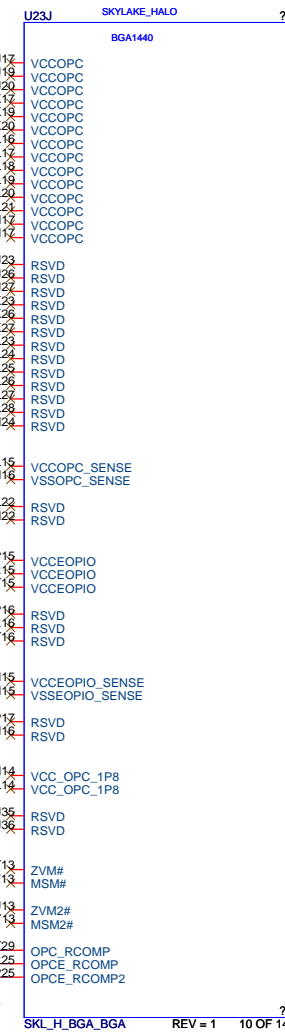
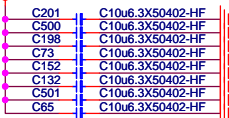
AG37 >>>VCCORE\_VCC\_SEN (45)

AG38 >>>VCCORE\_VSS\_SEN (45)

VCC\_SENSE  
VSS\_SENSE

SKL\_H\_BGA\_BGA REV = 1 7 OF 14

+VCC\_CORE



GT4 Power

GT4 Power

GT4 Power

?

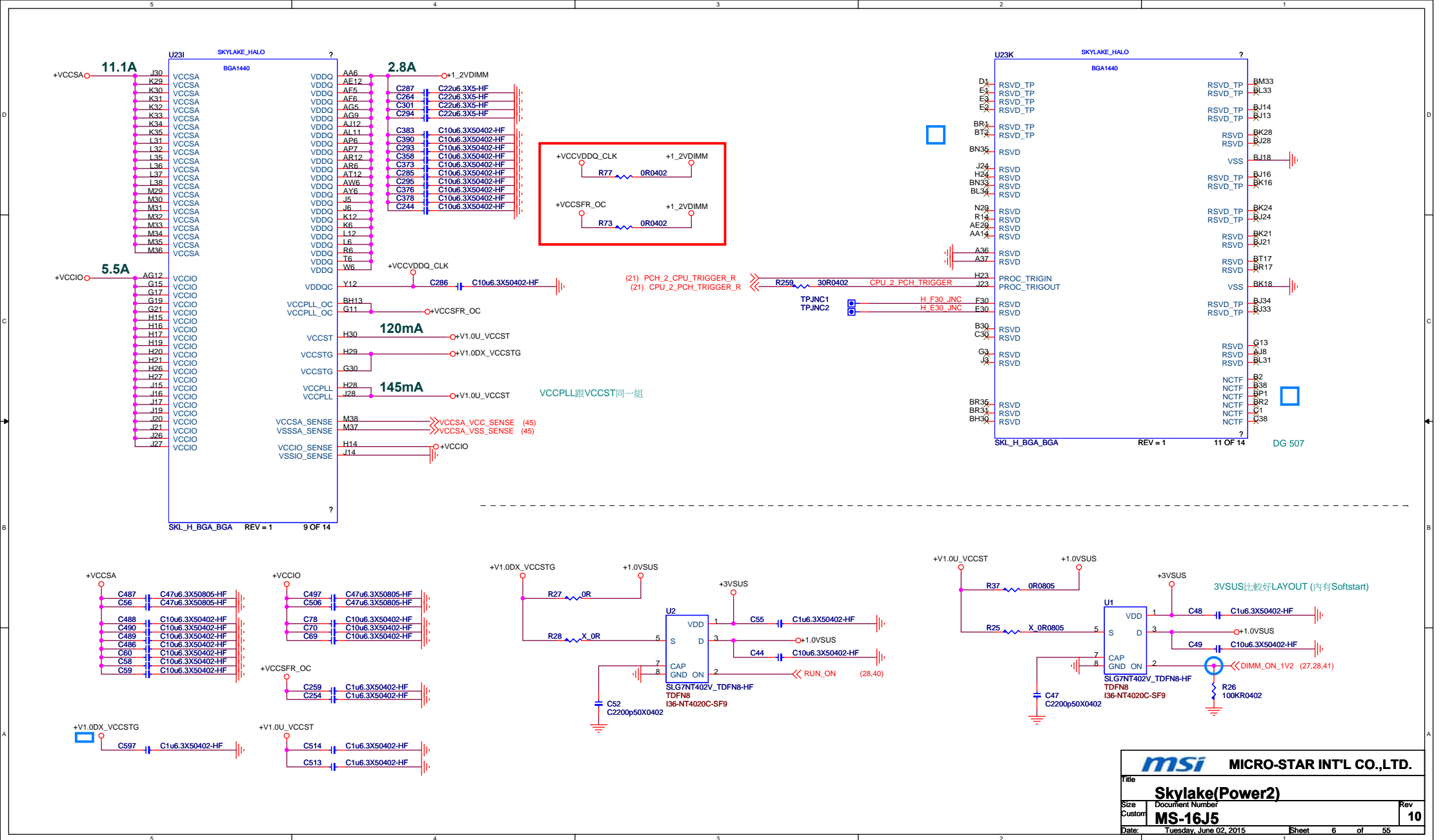


Unconnected for Processors without OPC. EDS.P121

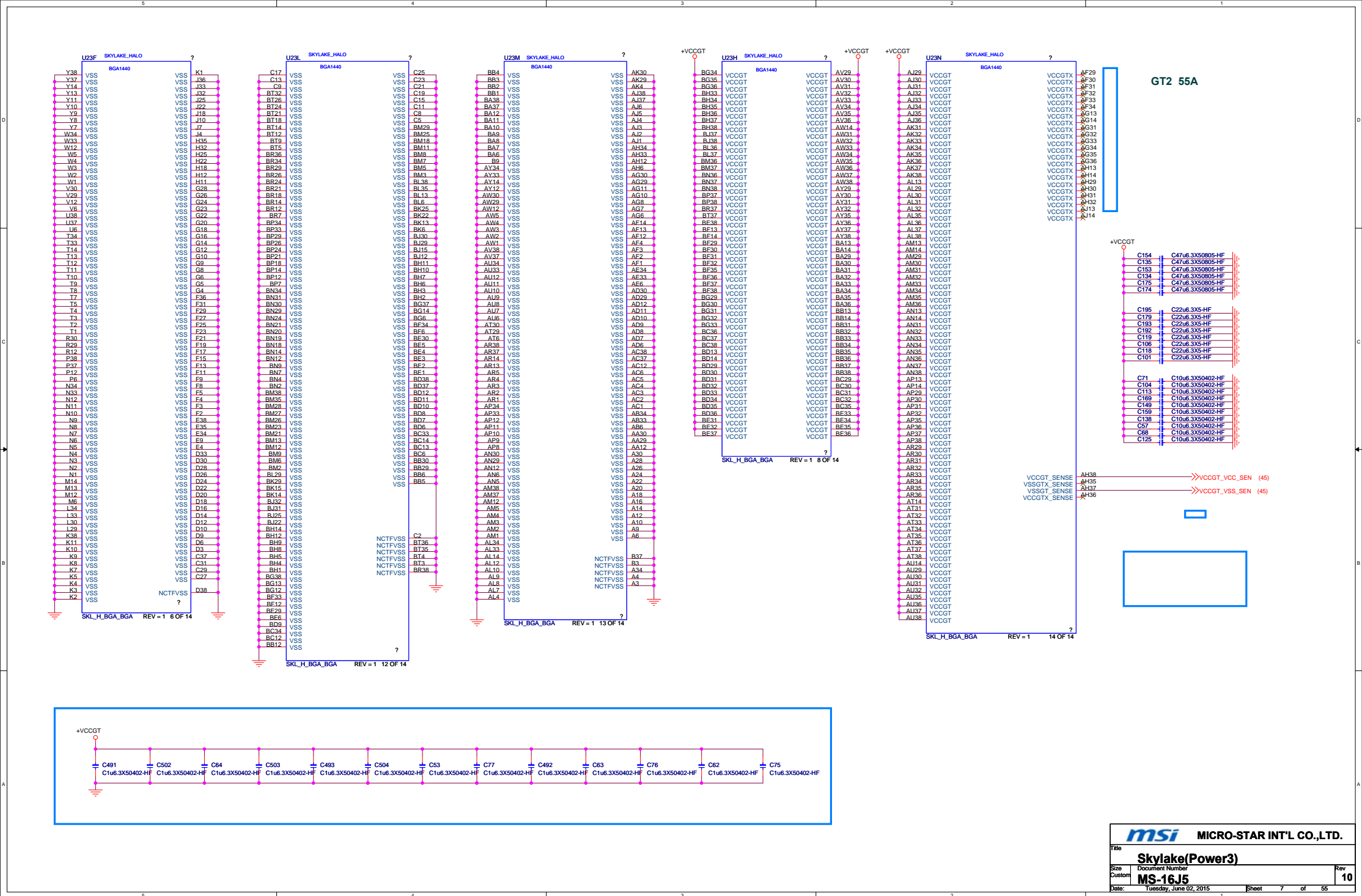
VCCGTx, VCCOPC, VCCOPC\_1p8, VCCEOP10 is only applicable to SKUs with OPC

SKL\_H\_BGA\_BGA REV = 1 10 OF 14



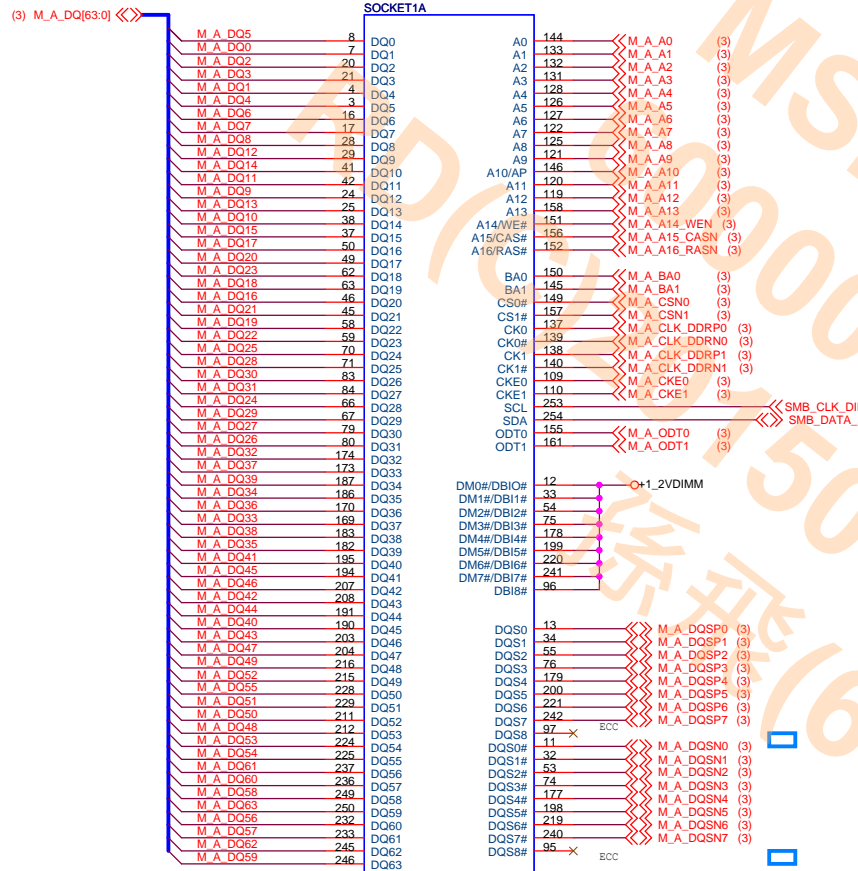




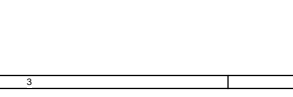
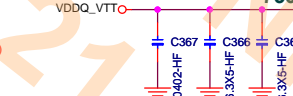
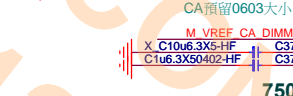
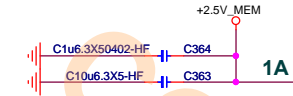




# SODIMM\_A0 (BOT-Reverse)



標準10UF x 2 / 1UF x 2 (刪除零件數)



msi MICRO-STAR INT'L CO.,LTD.		
Title		
DDR4 SODIMM A0		
Size	Document Number	Rev
Custom	MS-16J5	10
Date:	Tuesday, June 02, 2015	Sheet 8 of 55

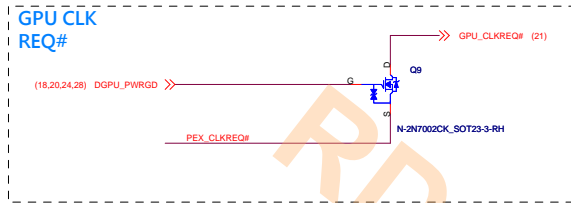


(3) M\_B\_DQ[63:0] <<>





N16P-GX( PCI-Express Gen3 x16 Interface)

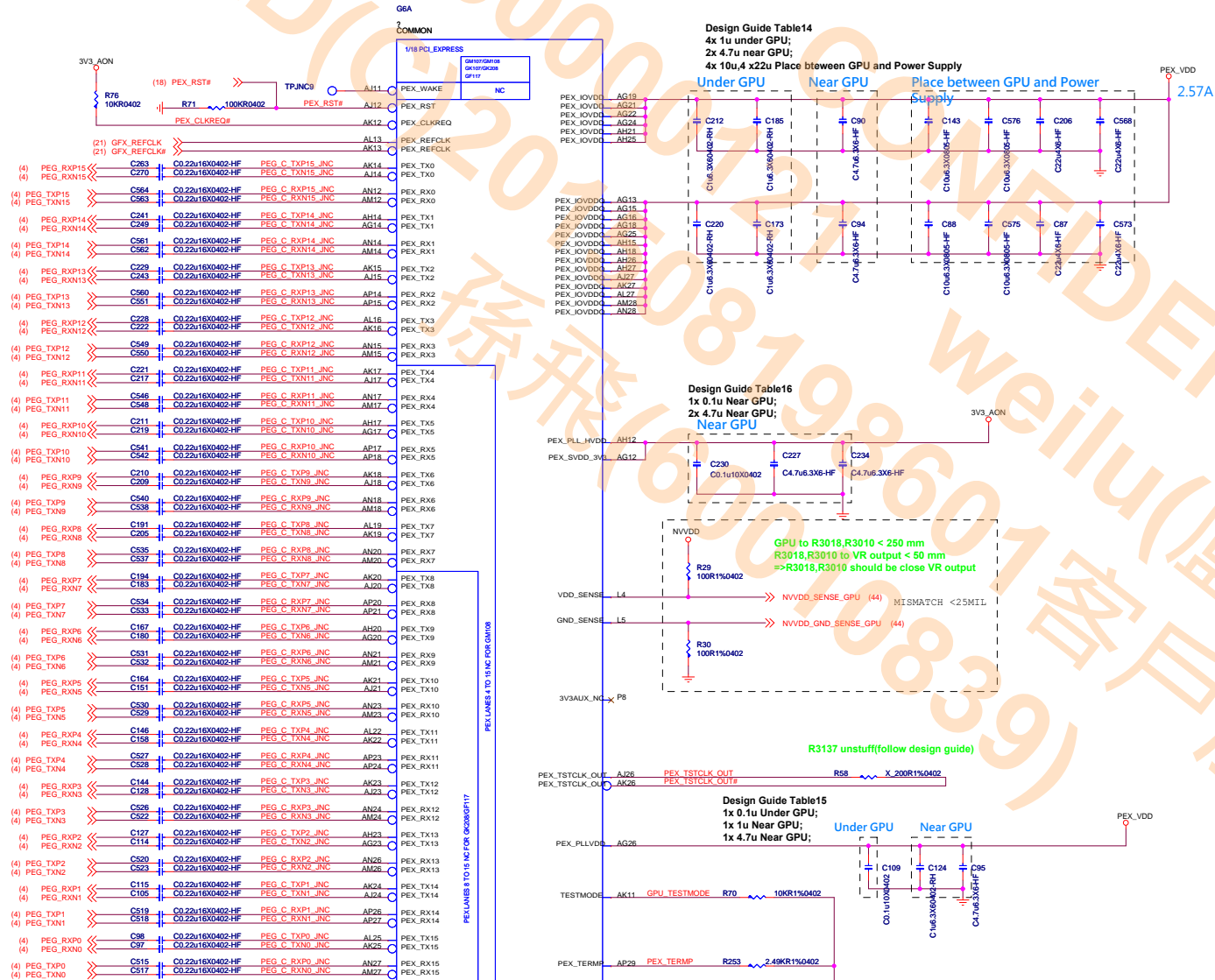


**GTX950**

**B03-0N16P05-N08**

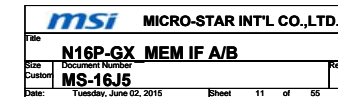
X\_N16P-GT-A2

5020



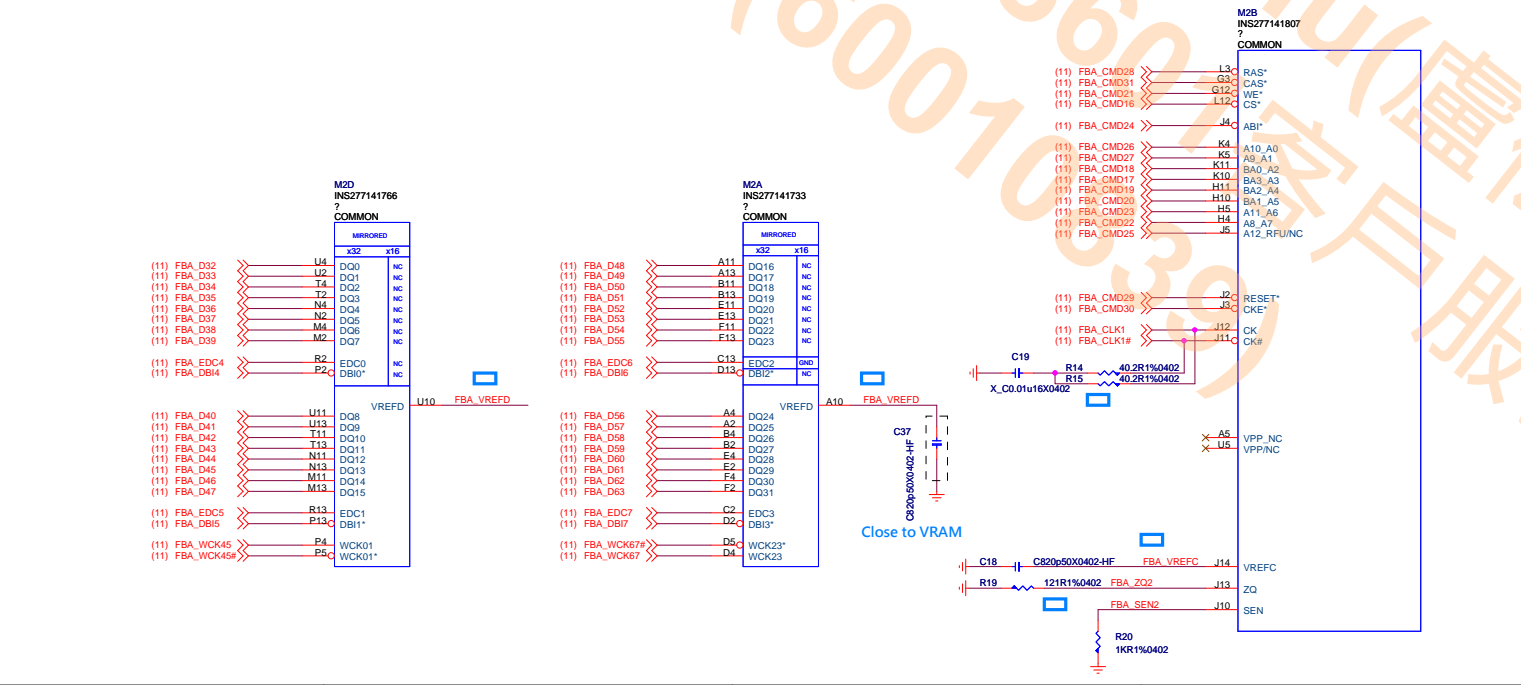
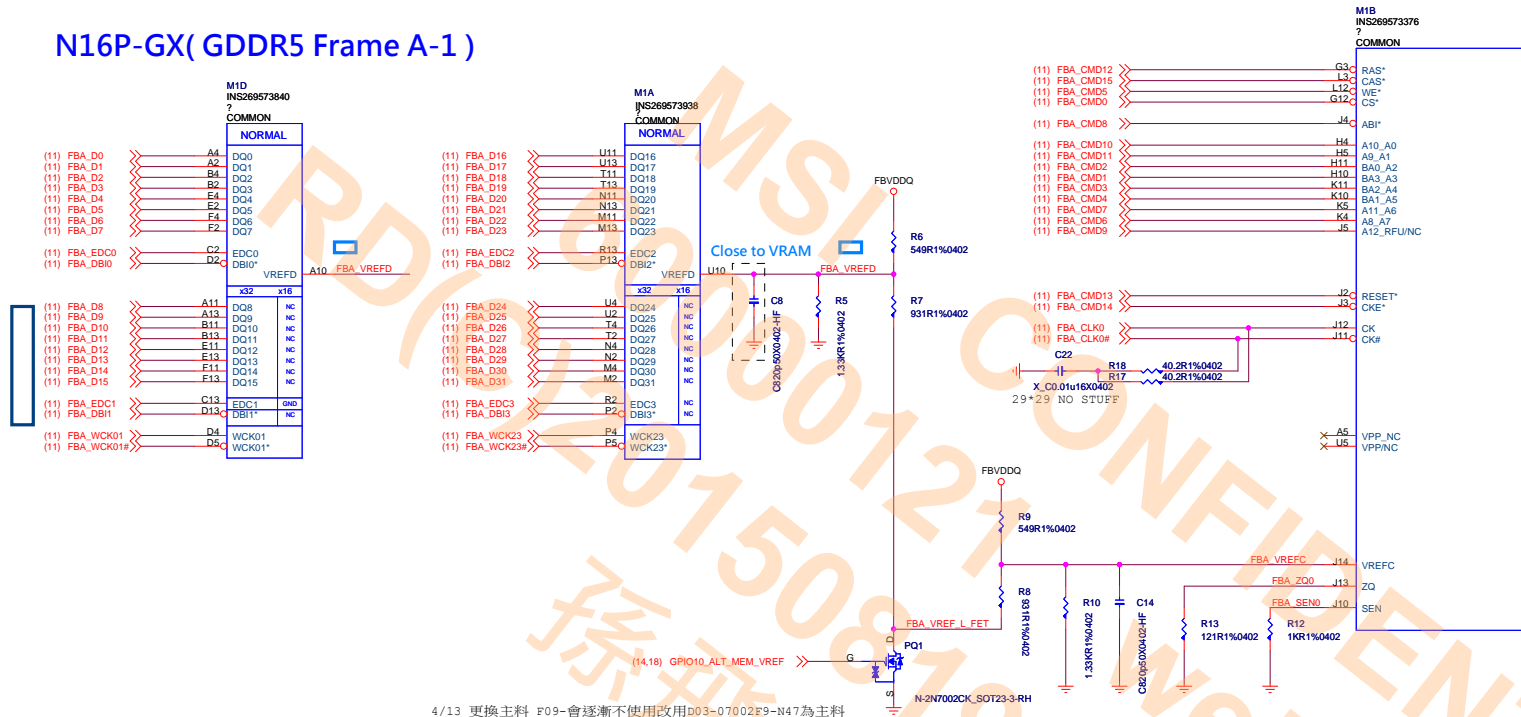


GC6M is GC6 2.0 that it is for N15x or later GPU  
So we use CRB GC6M design



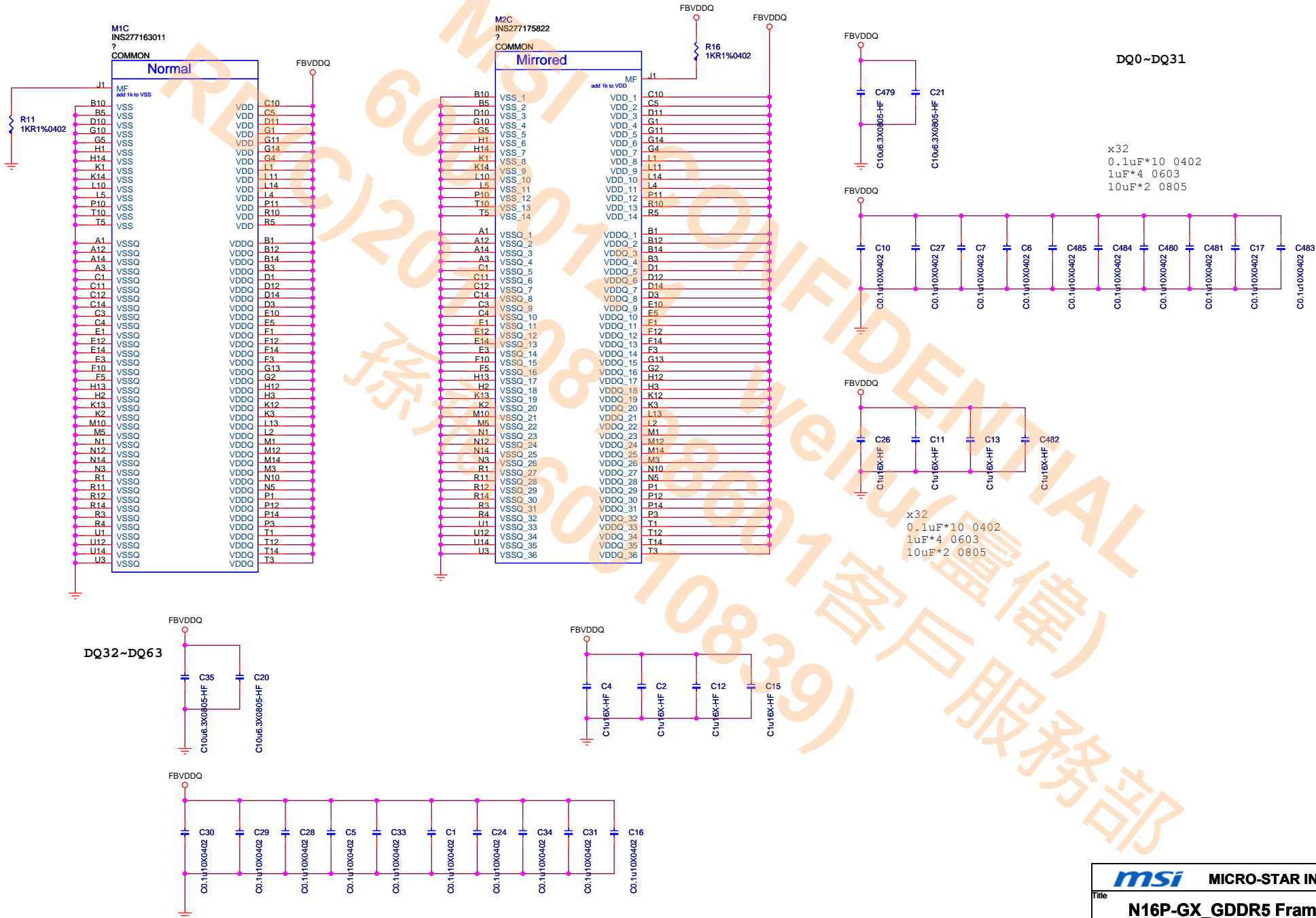


# N16P-GX (GDDR5 Frame A-1)



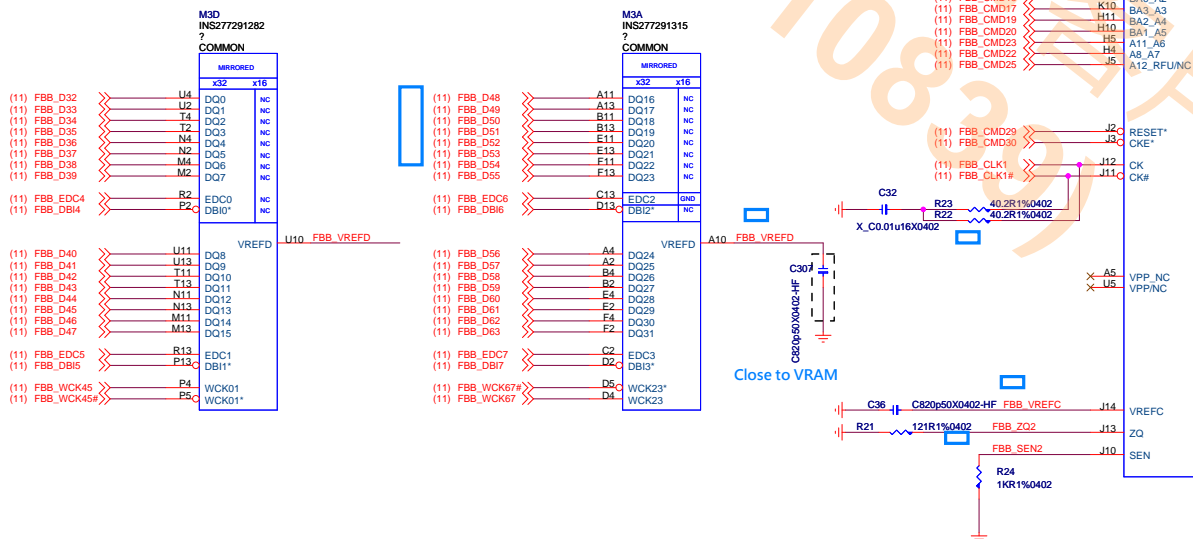
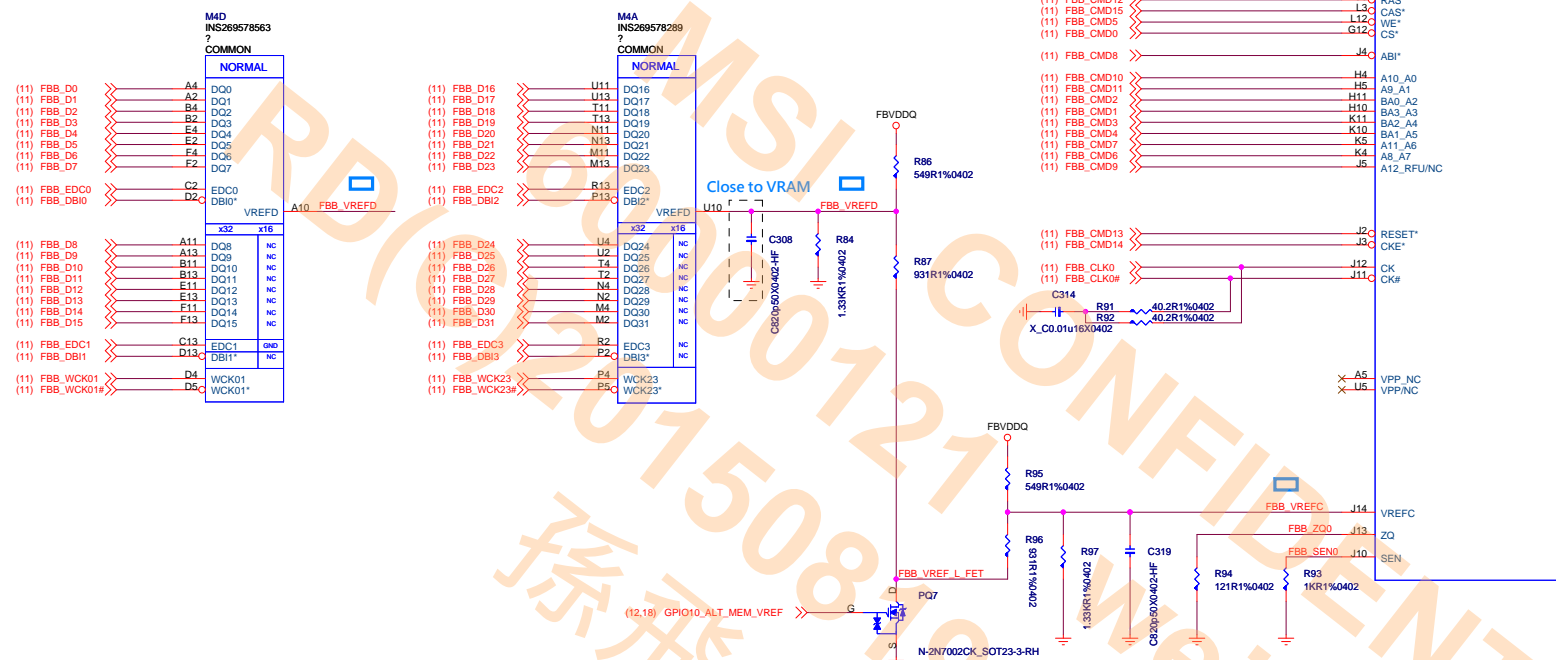


N16P-GX( GDDR5 Frame A-2 )



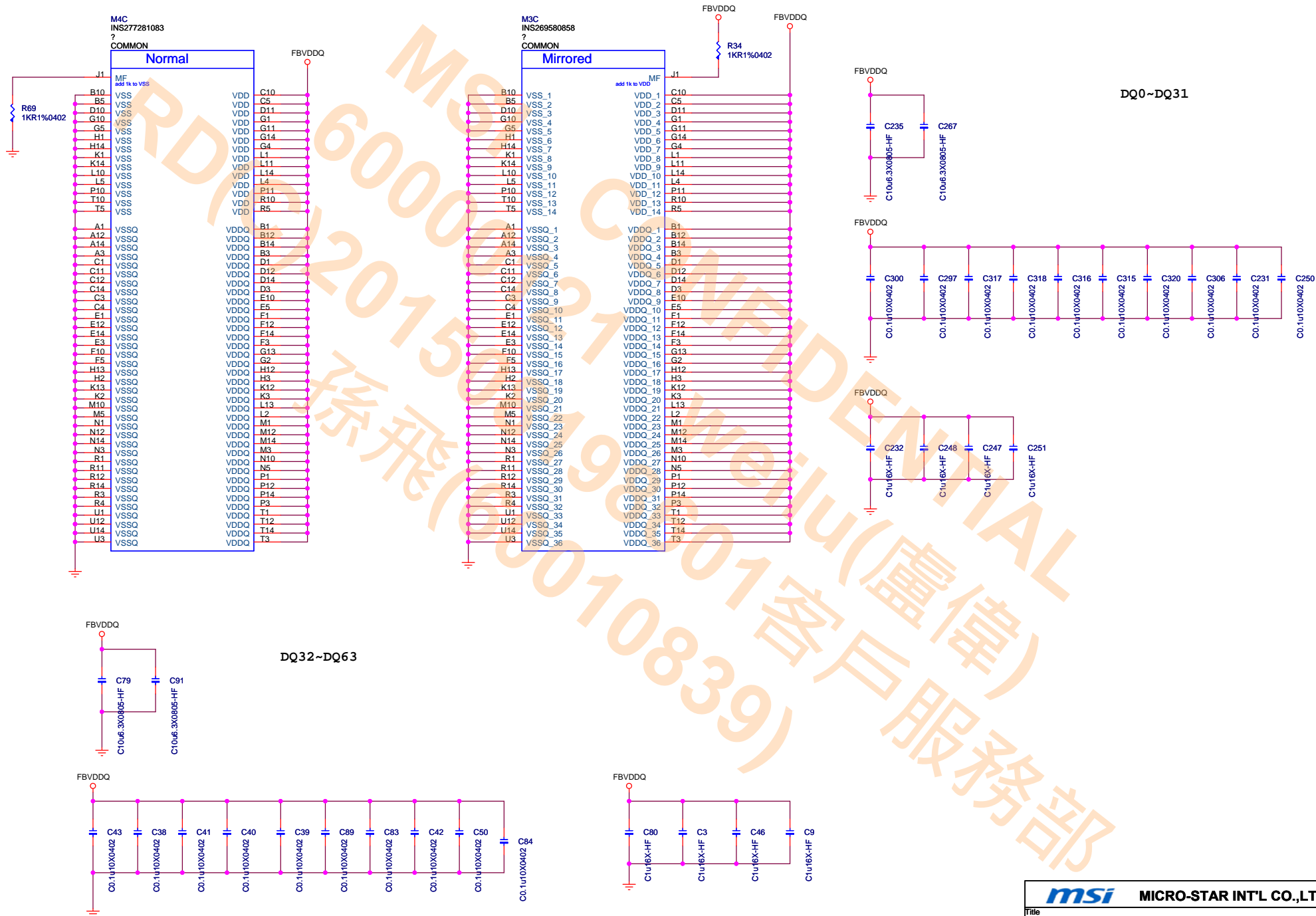


N16P-GX( GDDR5 Frame B-1 )





# N16P-GX( GDDR5 Frame B-2 )





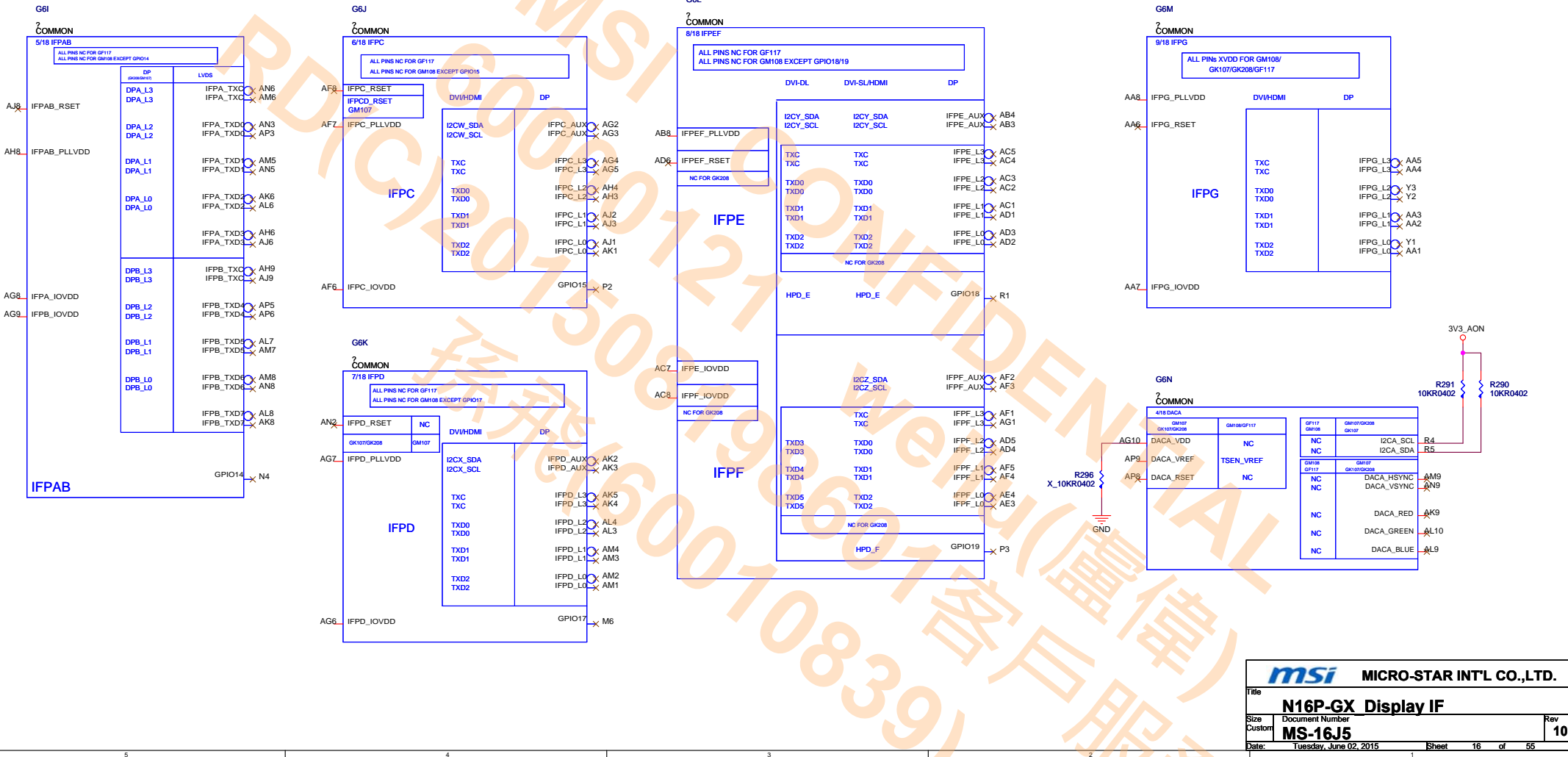
N16P-GX( Display IF)

IFP A/B LVDSDual Link

IFP C Native HDMI OR DP

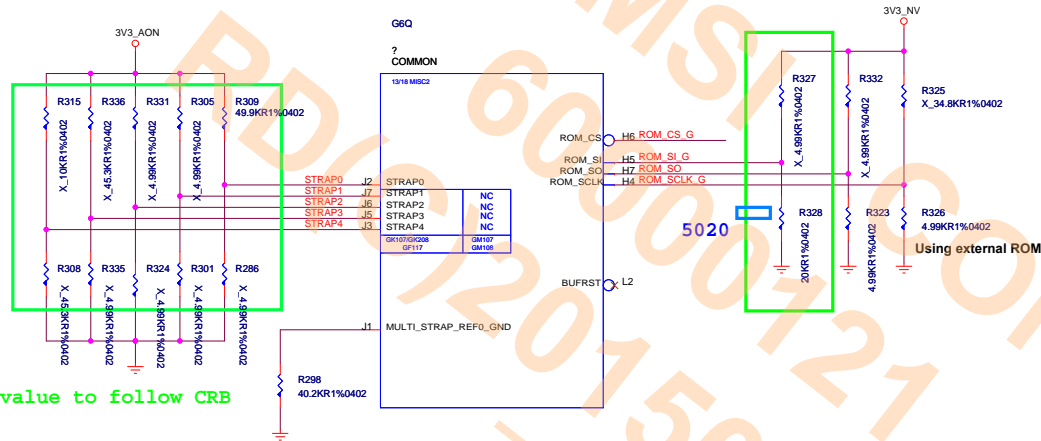
IFP E/F Dual Link TMDS DVI-I

DAC A VGA

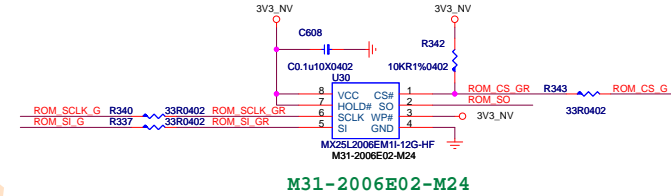




# ROM, MULTI-LEVEL STRAPS

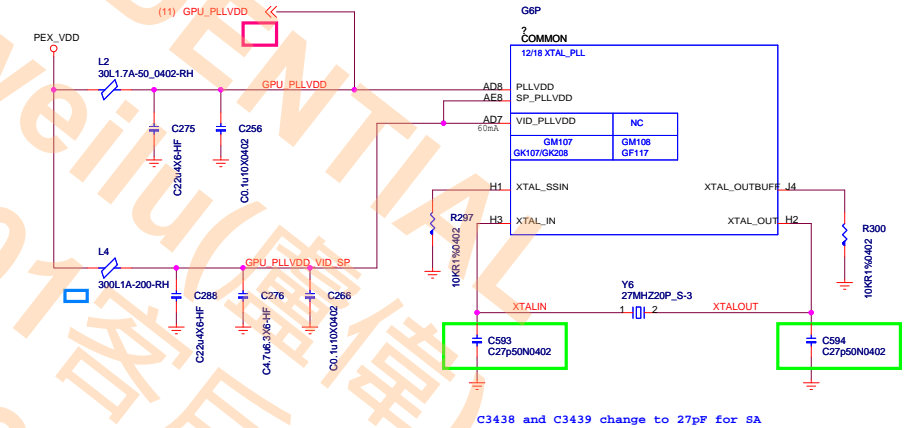


## External EEPROM



BOT 記得轉階層				BOT 記得轉階層			
DEFAULT SETTING							
ROM_S2	Samsung			V_BOT5	5020		
	128Mx32bit				M12-4132525-S02		
	R11-0203T12-W08	5020			X_K4G41325FC-HC03		
	X_20KR1%0402						
ROM_H2	Hynix			V_BOT4	5020		
	128Mx32bit				M12-5GC4H05-H23		
	R11-0153T12-W08	5020			X_H5GC4H24MFR-T2C		
	X_15KR1%0402						
ROM_M2	Micron			V_BOT6	5020		
	128Mx32bit				M12-4032B05-E59		
	R11-2492T12-W08	5020			X_EDW4032BABG-60-F-HF		
	X_24.9KR1%0402						
ROM_H3	Hynix			V_BOT7	5020		
	128Mx32bit				M12-5GC4H65-H23		
	R11-3482T12-W08	5020			X_H5GC4H24AJR-T2C		
	X_34.8KR1%0402						

ROM_SI	RAM_CFG[3:0]	
<div> <div>Micron GDDR5 : M12-4032B05-E59</div> <div>Samsung GDDR5 : M12-4132525-S02</div> <div>Hynix GDDR5 : M12-5GC4H05-H23</div> <div>Hynix GDDR5 : M12-5GC4H65-H23</div> </div>		
ROM_SO	DEVID_SEL	5K PD
	PCIE_CFG	
	SMB_ALT_ADDR	
	VGADEVICE	
ROM_SCLK	SOR_EXposed[3:0]	5K PD
STRAP0		50K PU 3V3_AON
STRAP1		Reserved
STRAP2		Reserved
STRAP3		Reserved
STRAP4		Reserved



	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

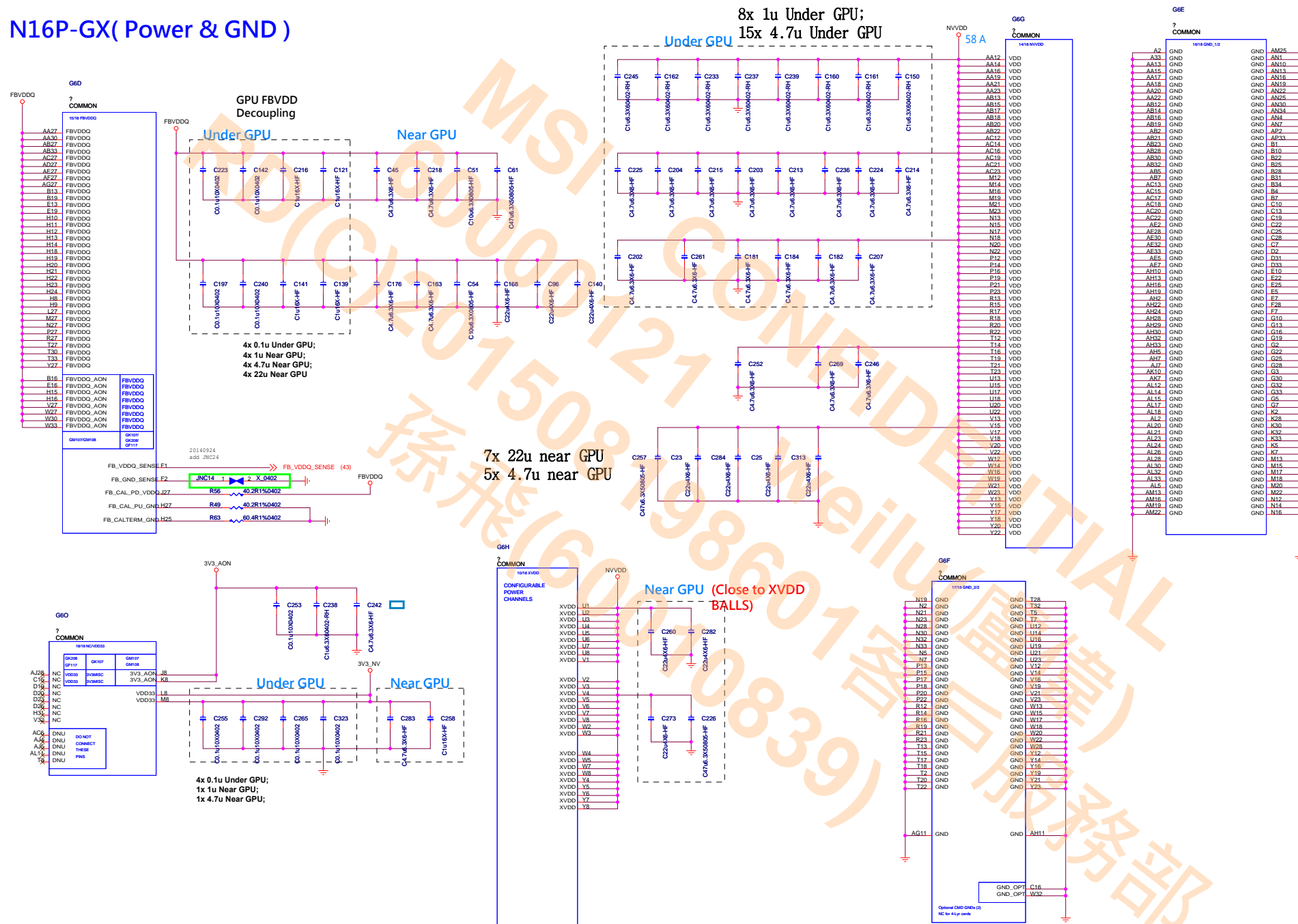






## N16P-GX( Power & GND )

8x 1u Under GPU;  
15x 4.7u Under GPU



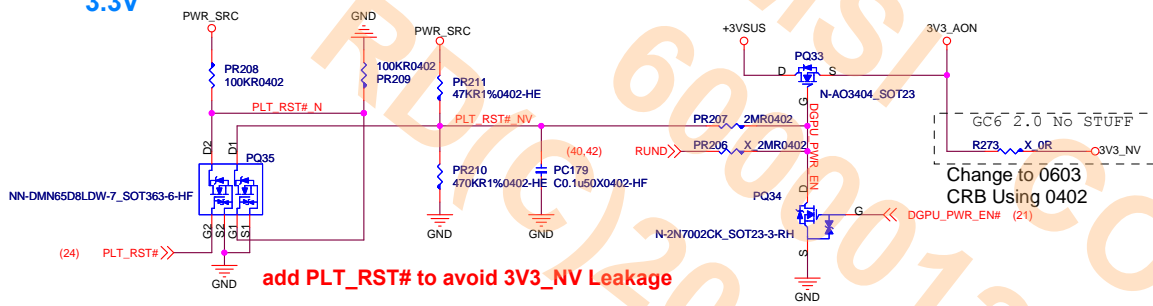


# N16P-GX( Power Control )

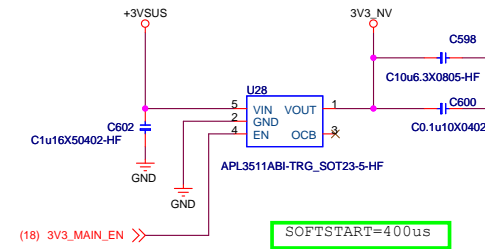
## nVIDIA Power Sequence Control

3V3\_AON -> 3V3\_NV -> NVVDD -> PEX\_VDD -> FBVDDQ -> DGPUPWRGD

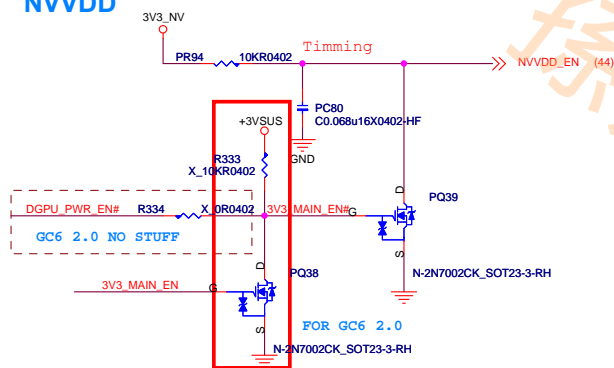
### 3.3V



### GC6 2.0 STUFF



### NVVDD

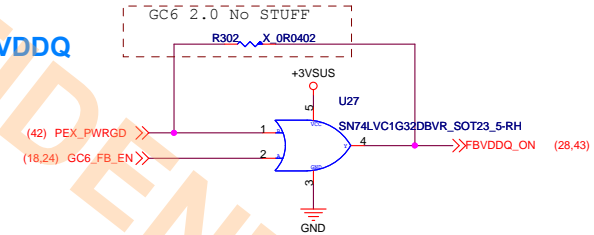


### PEX\_VDD

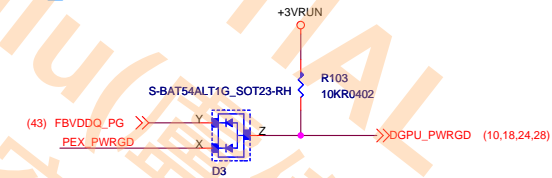
EDP Design Guide:  
N16P-GX  
NVVDD : 51.1A ; Peak 87A  
3.3VRUN : 0.34A  
PEX\_VDD : 2.57A  
FBVDDQ : 8.75A

EDP Design Guide:  
N16P-GT  
NVVDD : 30.2A ; Peak 53A  
3.3VRUN : 0.34A  
PEX\_VDD : 2.57A  
FBVDDQ : 8.75A

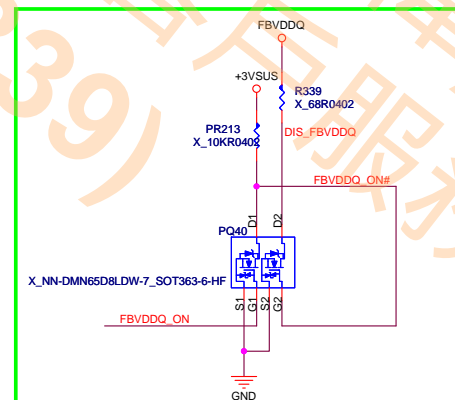
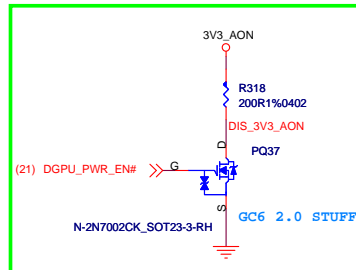
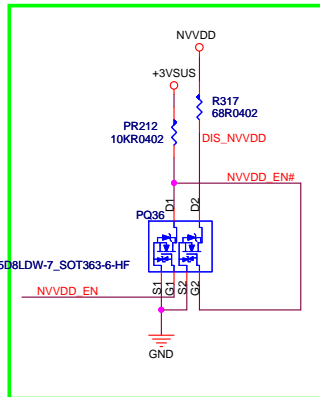
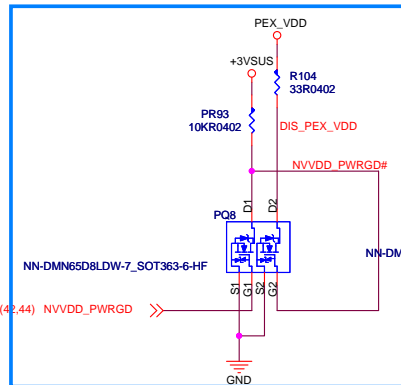
### FBVDDQ



### DGPU\_PWRGD



### Discharge Circuit



4/13更換料號  
D03-7002D10-D07 轉到 D03-65D8109-D07



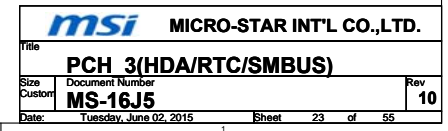








PCH EDS Page 52







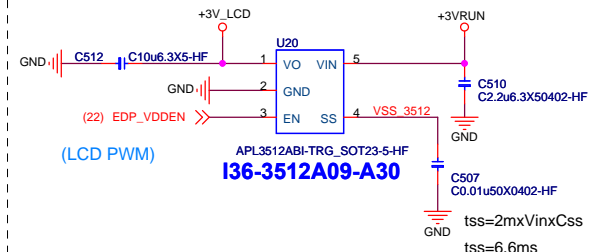




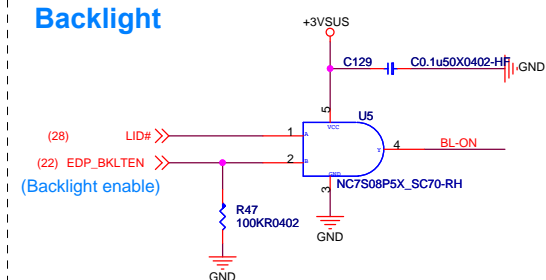


## eDP

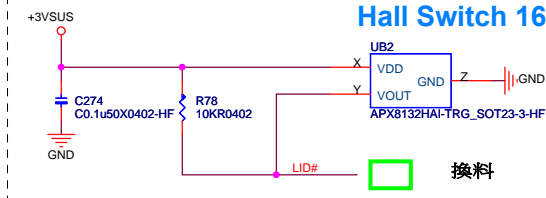
### Pannel Device Logic Power



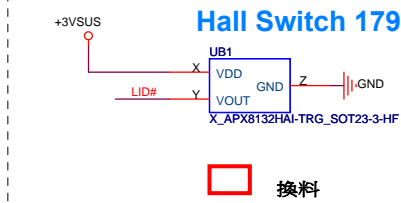
### Backlight



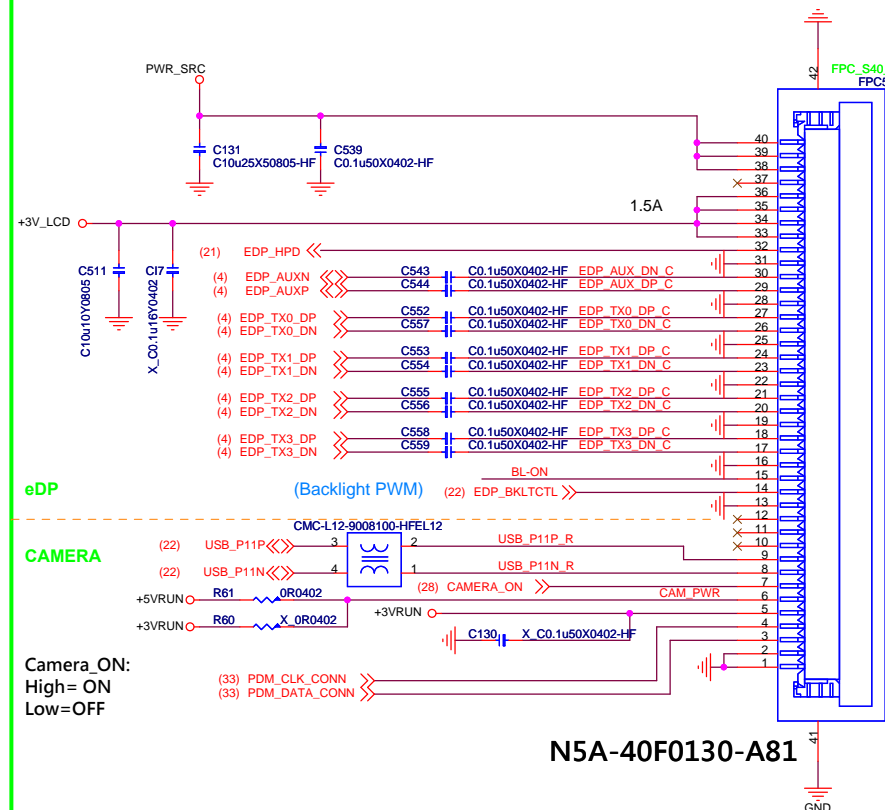
### Hall Switch 16J5



### Hall Switch 1795

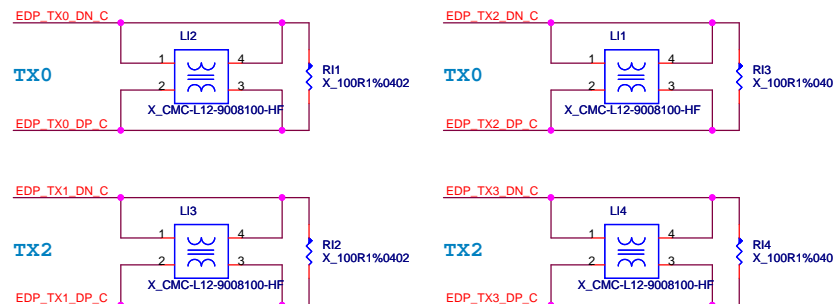


## eDP CONN CAMERA



## LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon



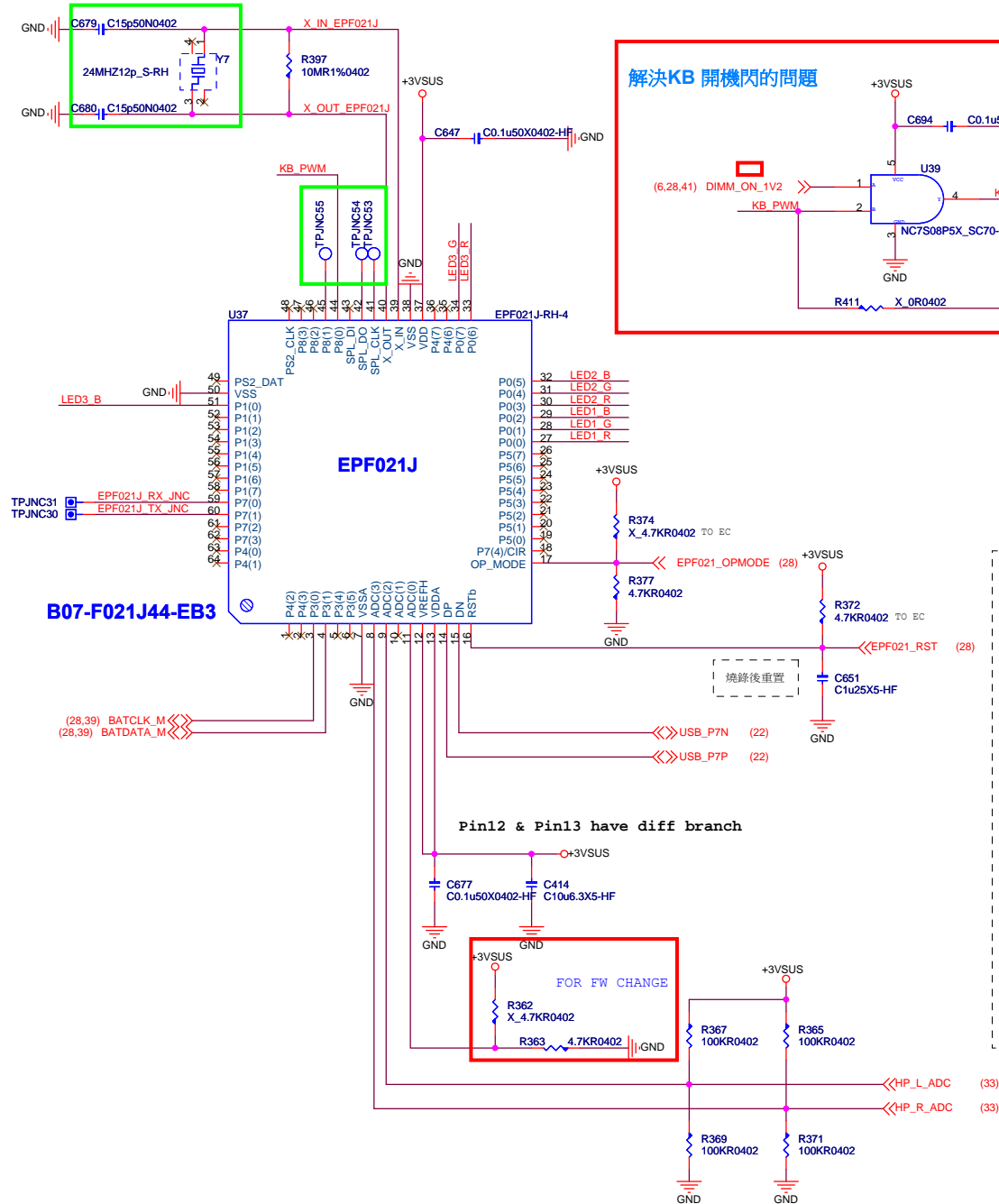
Place Close eDP Connector

Reserve for EMI

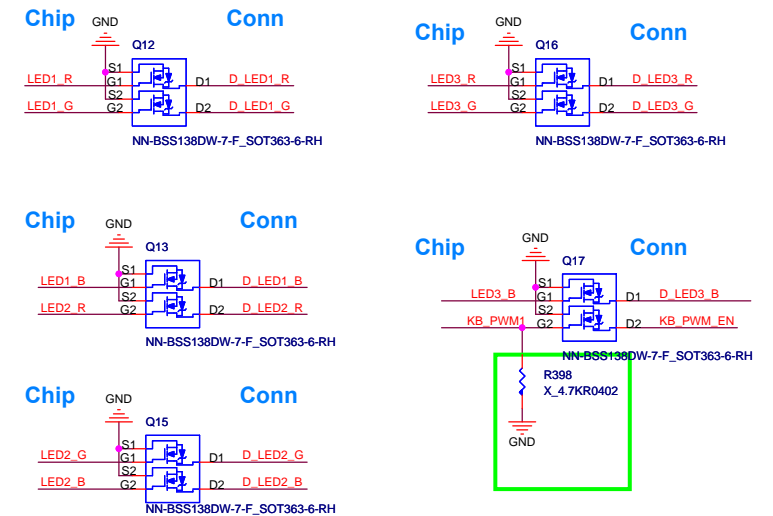


# LED 8051 Controller

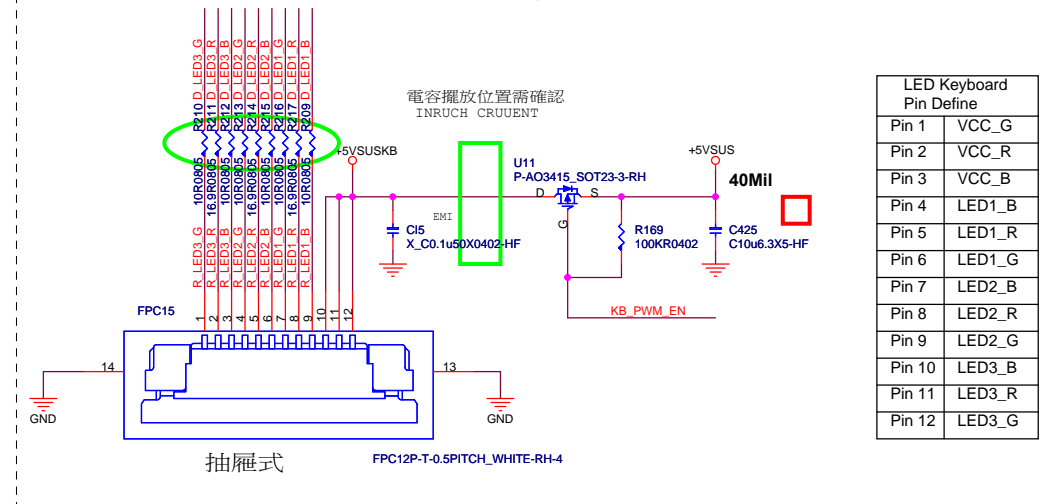
C749 and C750 change to 15pF for SA



**EPF021J Sink current not enough, only using BSS138 (0.22A)**



## LED Keyboard CONN

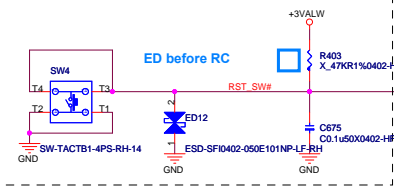


LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

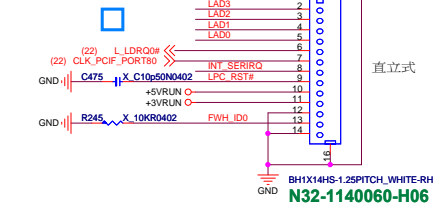


# KBC/EC/uP (ENE9028)

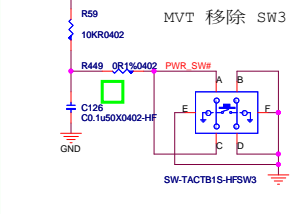
## Hardware Reset



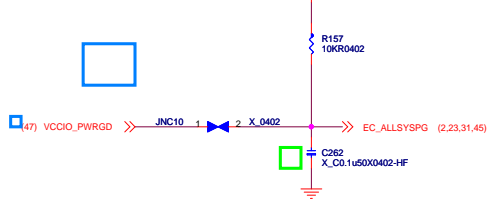
## SW Debug (LPC)



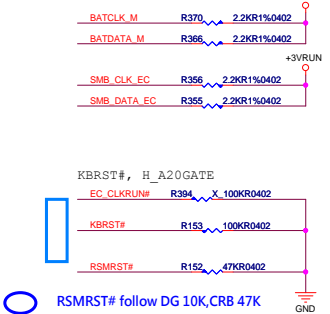
## HW Debug



## ALLSYSPG



## PU/PD

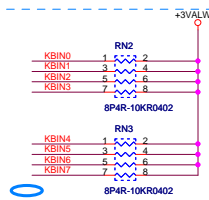
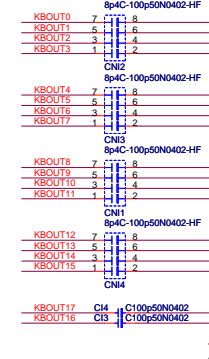
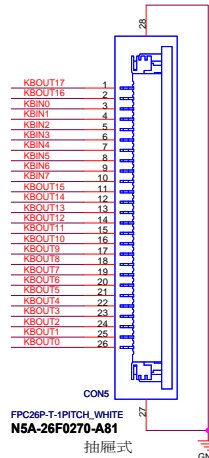


## SERIES\_ID



PR225	R146	Series
10.2K	X	GE
10.2K	31.6K	PE
10.2K	12.1K	GP

## Keyboard conn

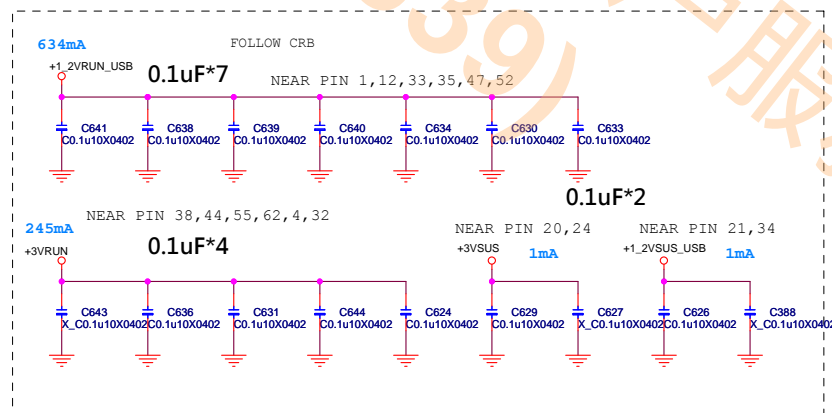
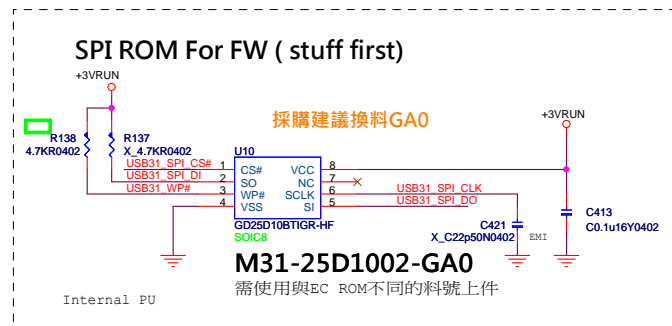


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File KBC/ (KB3930QFB1)  
Size Document Number MS-16J5  
Date Tuesday, June 02, 2015 Sheet 28 of 55



## PCIE to USB 3.1







10



PC



## (22) I



## j-C



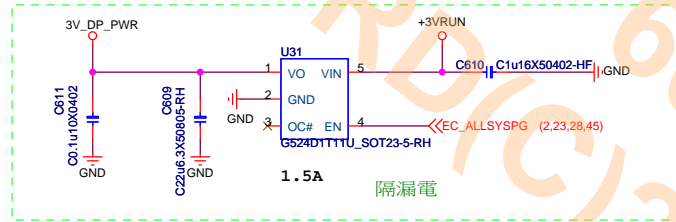


## Display Port

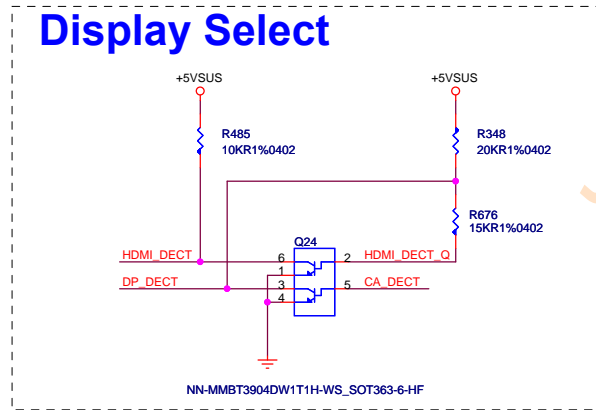
The preset trip limit must not exceed 3A at the Upstream device connector DP\_PWR pin and 1.5A at the Downstream device connector DP\_PWR pin.

ESD Contact  $\pm 5$  KV & Air  $\pm 15$  KV

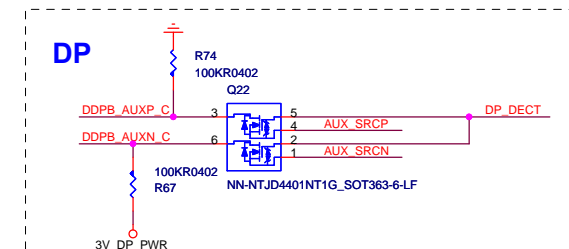
## Display Port



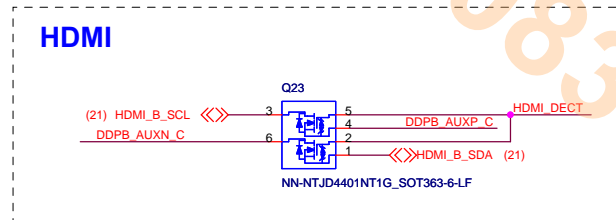
## Display Select



## Dual Mode Switch



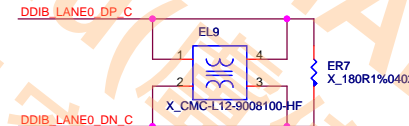
## HDMI



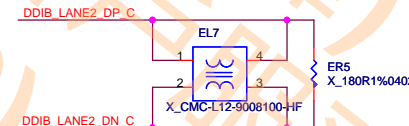
(4) DDPB\_AUXP C628 C0.1u50X0402-HF AUX\_SRCPC  
(4) DDPB\_AUXN C632 C0.1u50X0402-HF AUX\_SRCN

## EMI Close Connector

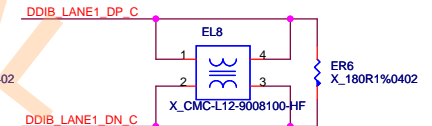
### LANE0



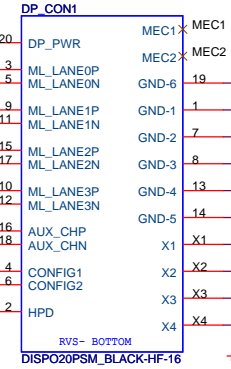
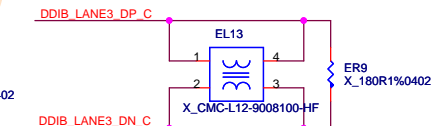
### LANE2



### LANE1

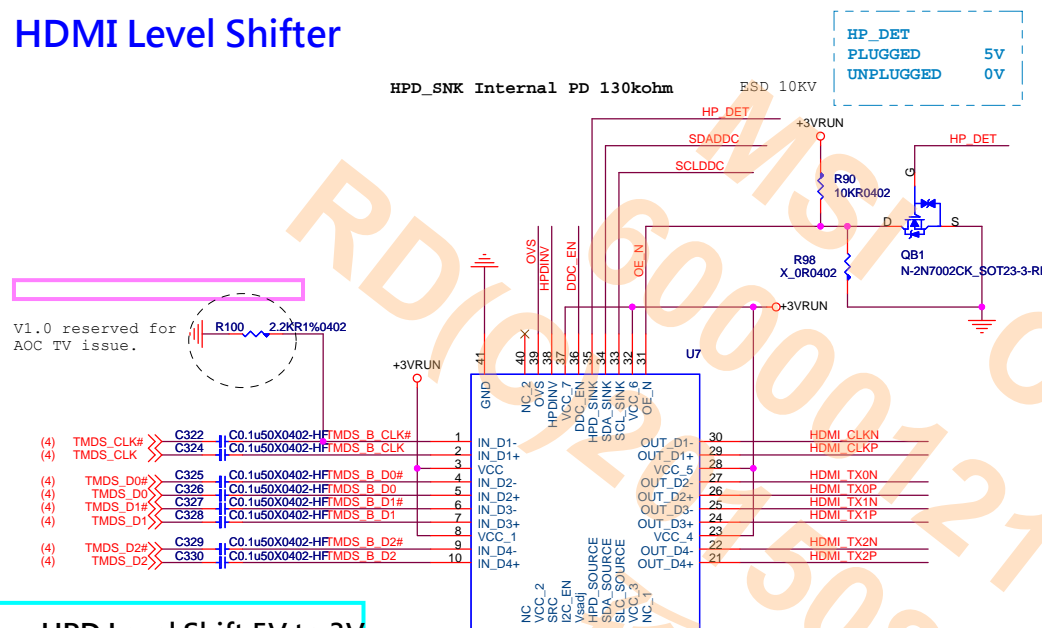


### LANE3

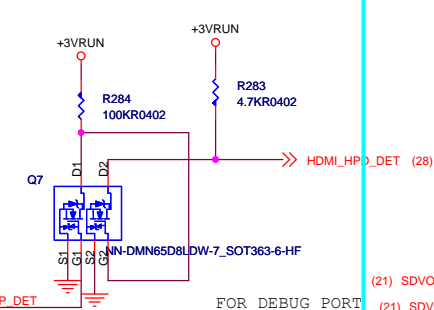




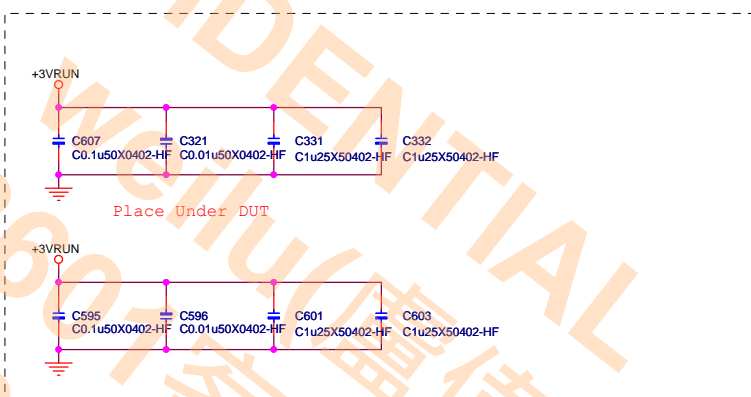
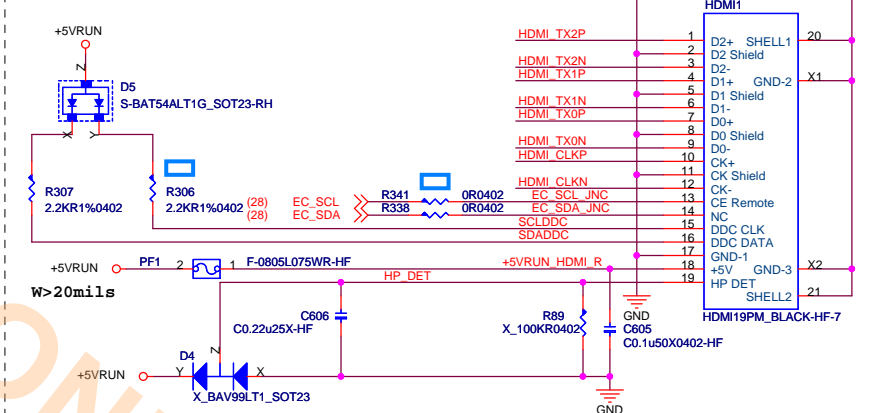
## HDMI Level Shifter



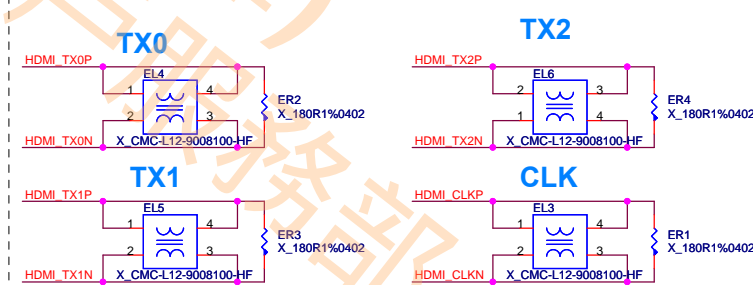
## HPD Level Shift 5V to 3V



## HDMI Connector



## EMI Close Connector

 MICRO-STAR INT'L CO., LTD.

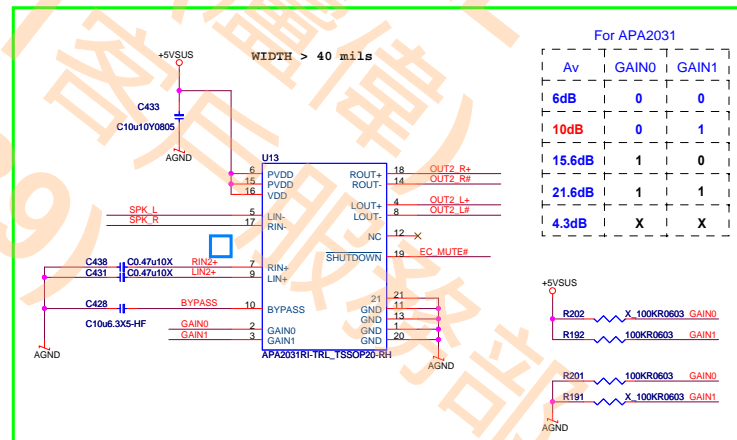
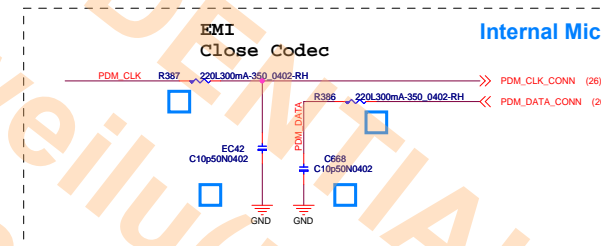
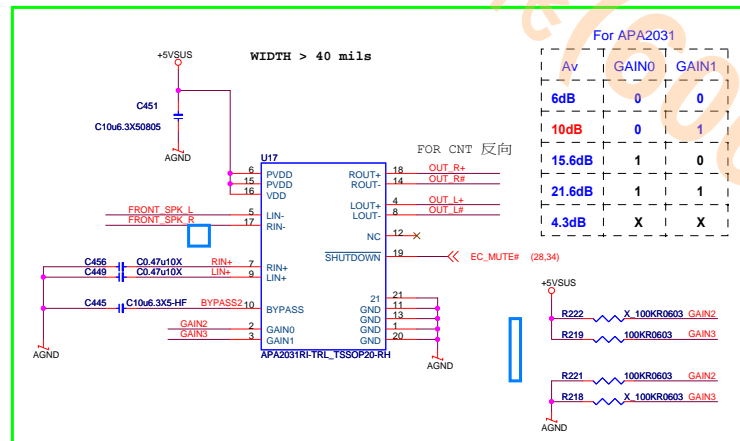
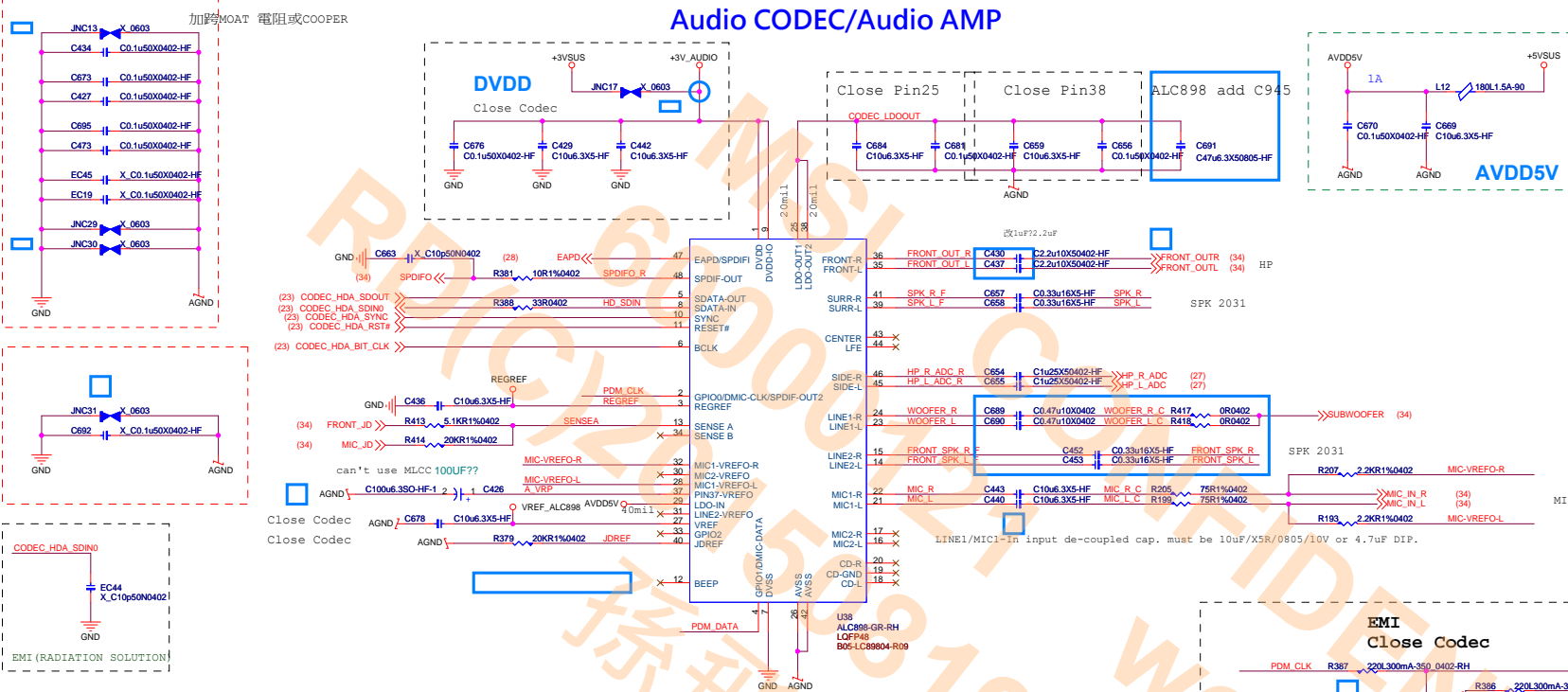
Title	HDMI DP139
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Size	Document Number	Re
	<b>MS-16.15</b>	

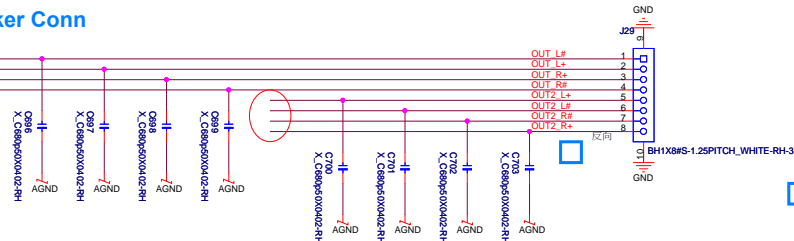
Date: Tuesday, June 02, 2015 Sheet 32 of 59



## Audio CODEC/Audio AMP



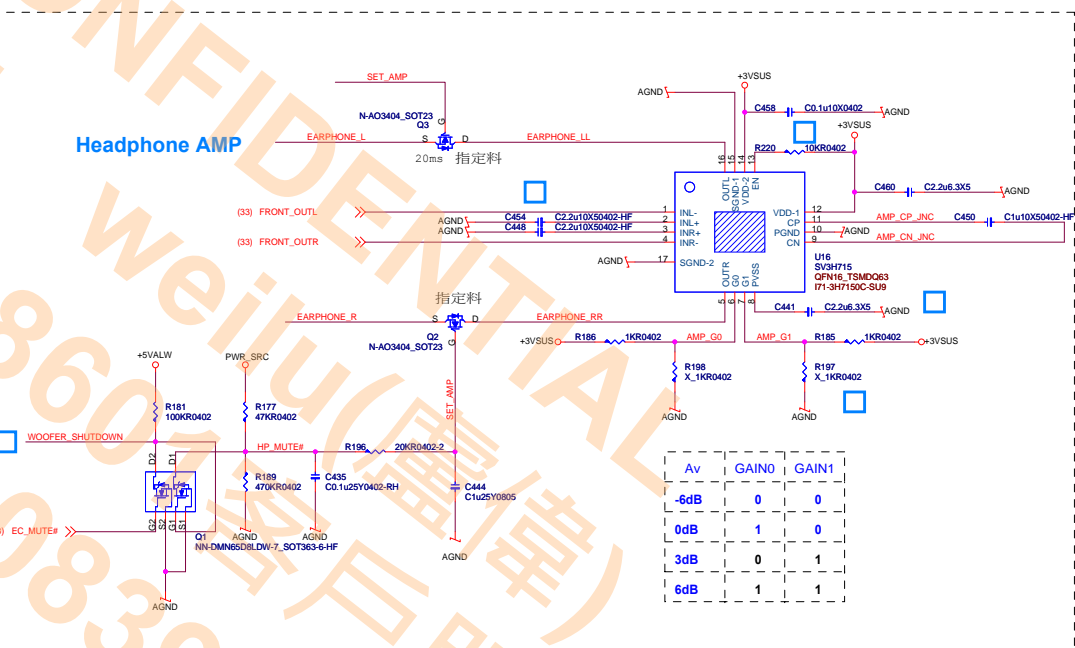
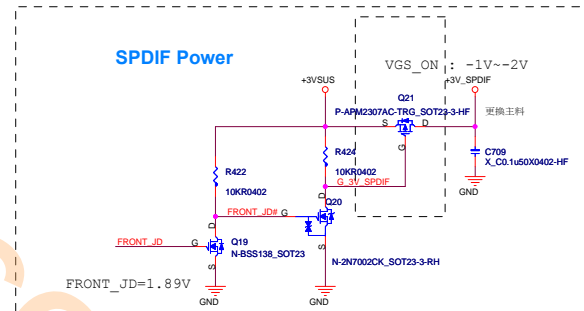
### Internal Speaker Conn



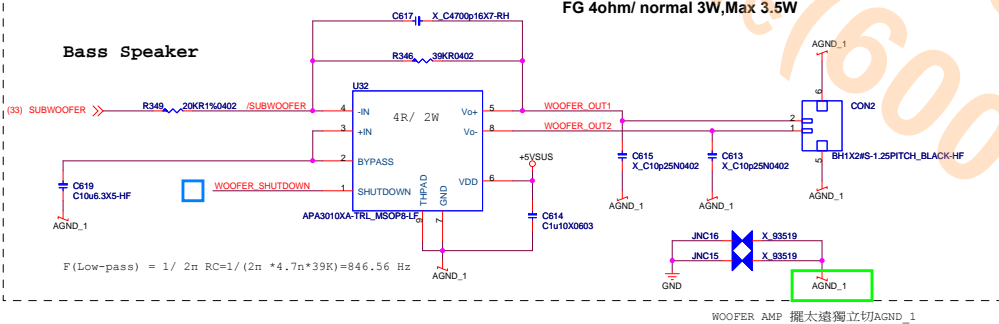
	CODEC	喇叭
L	-	-
L	+	+
R	+	+
R	-	-
L2	+	+
L2	-	-
R2	-	-
R2	+	+



FRONT OUT



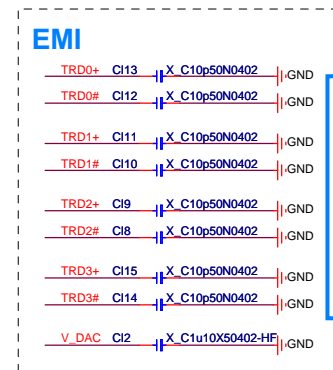
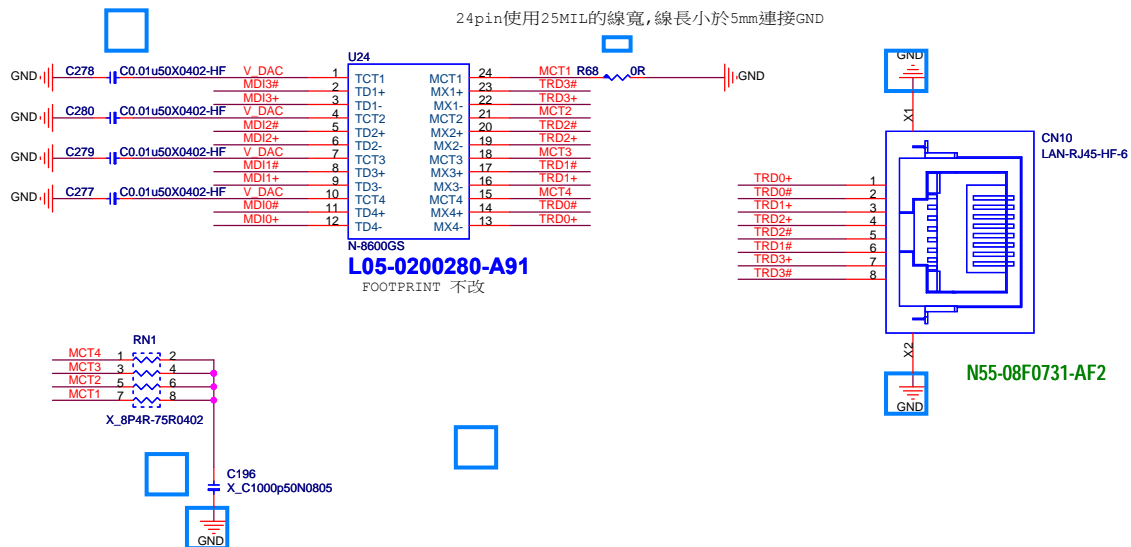
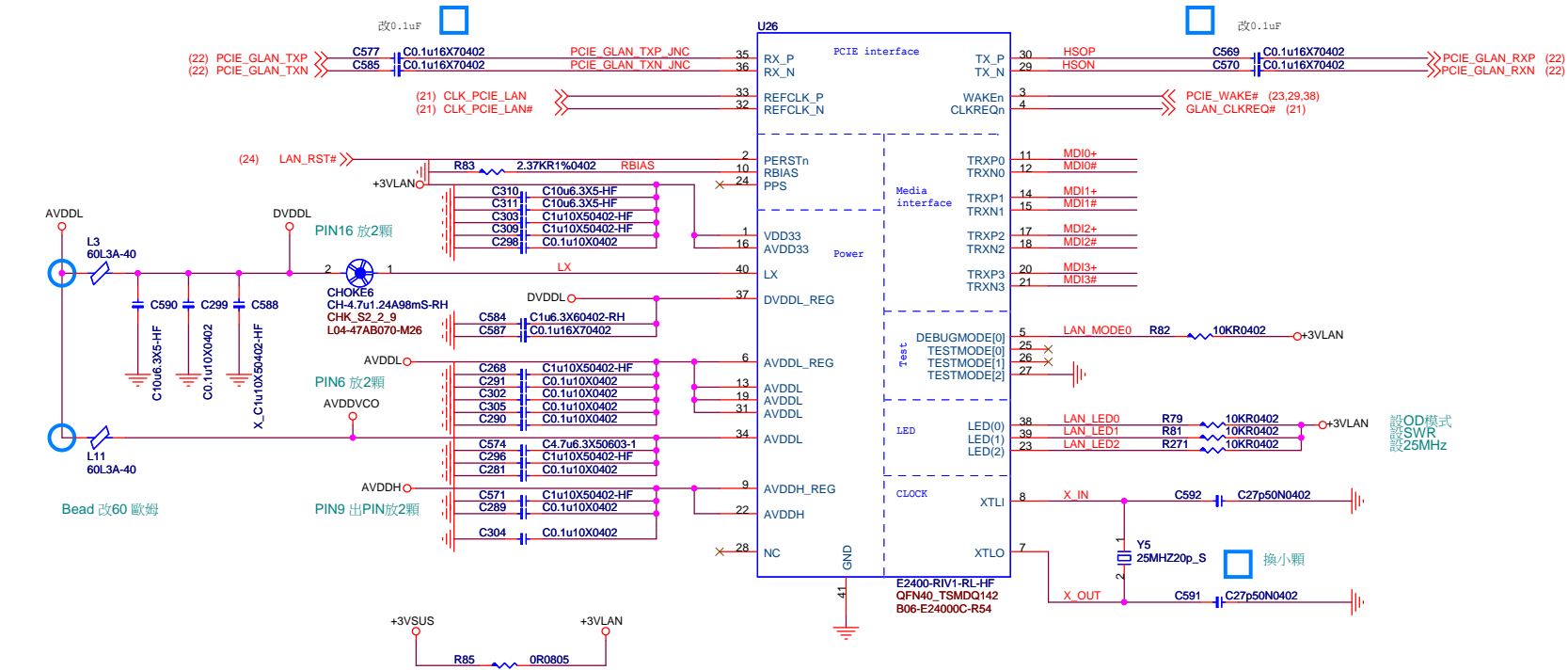
**Woofers SPEC**  
**YG 3.8ohm / normal 3W,Max 3.5W**  
**FG 4ohm/ normal 3W,Max 3.5W**



Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

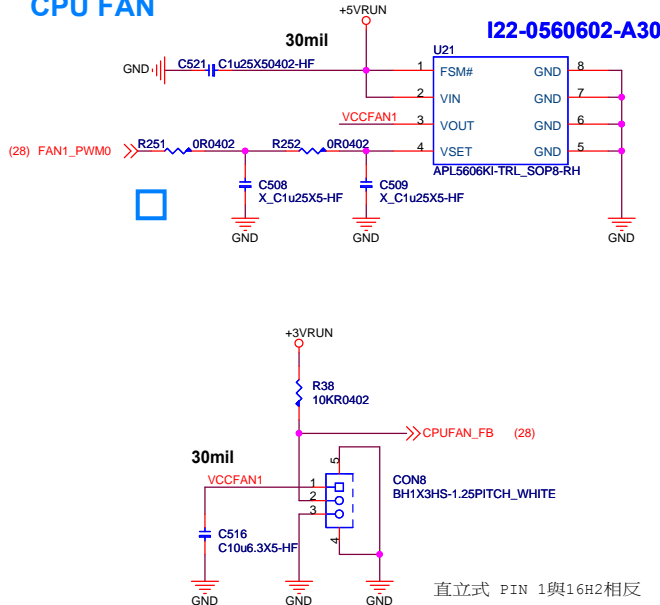


**GIGA LAN(BigFoot BFN2400B)**

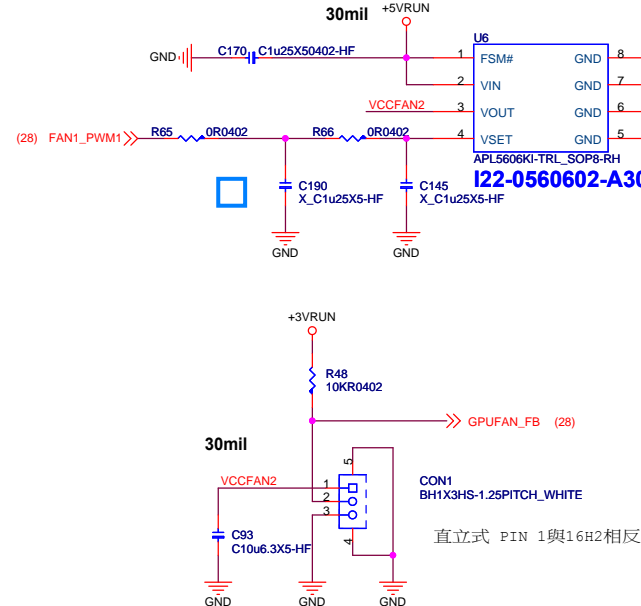




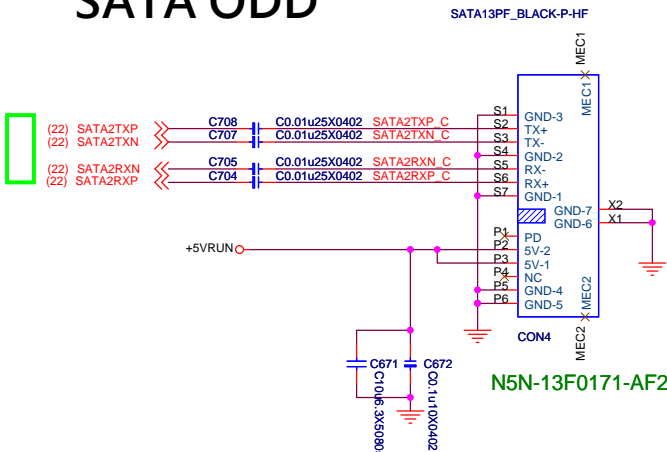
## CPU FAN



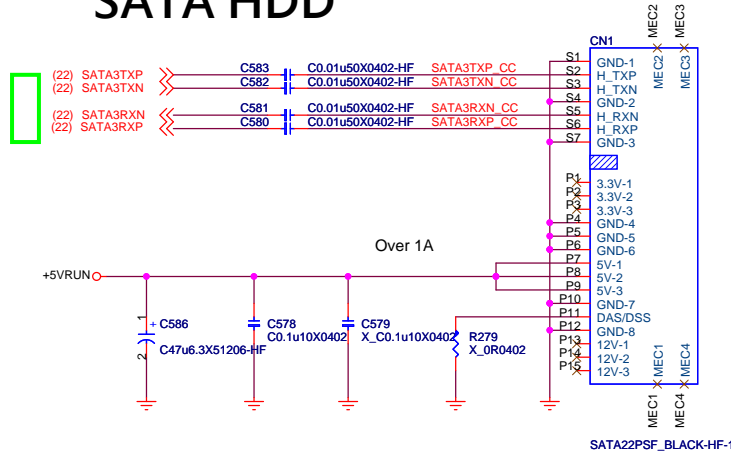
## DGPU FAN



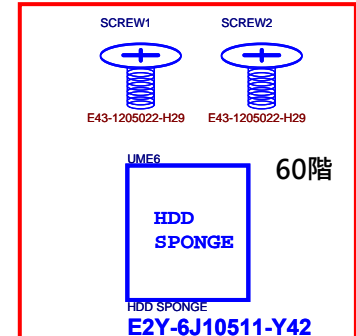
# SATA ODD



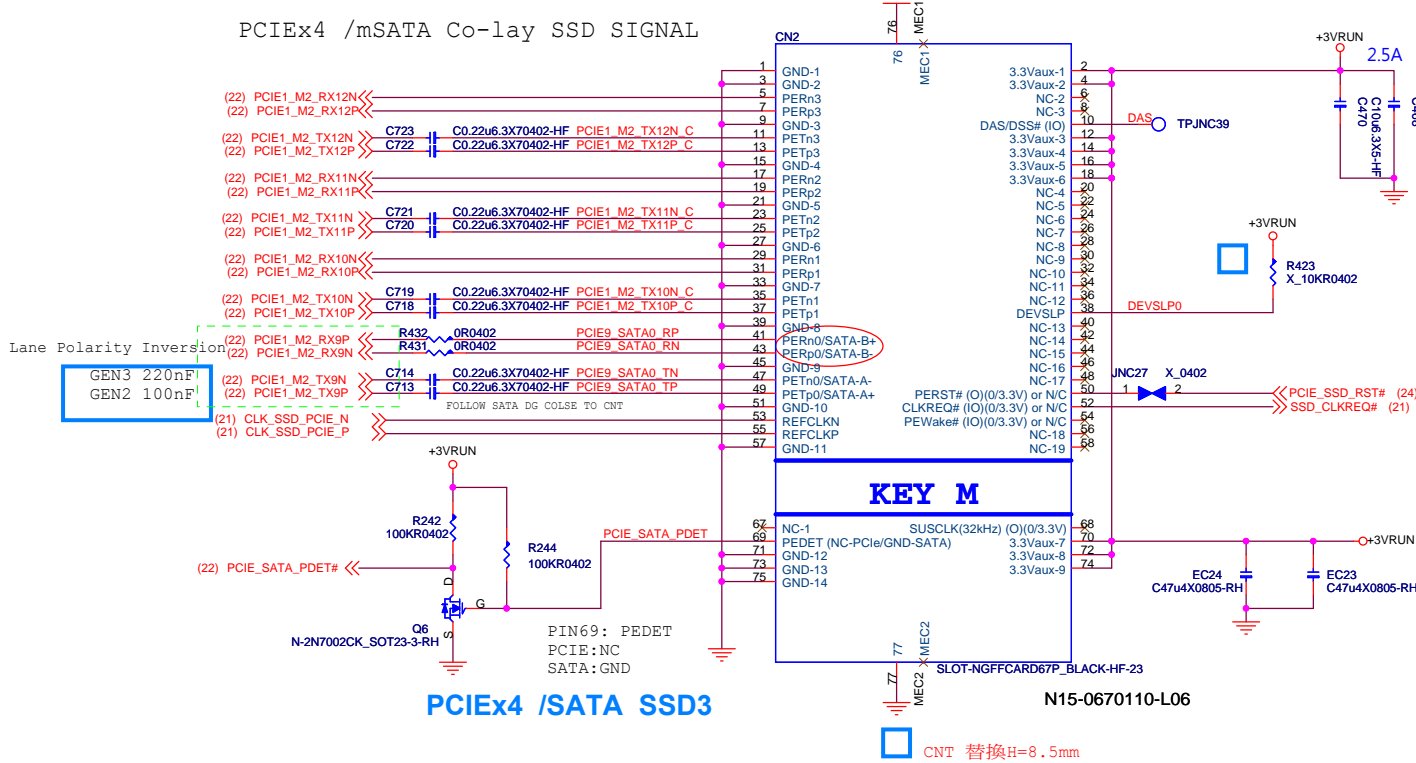
## SATA HDD



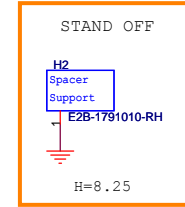
- 22.GND  
21.TX  
20.TX#  
19.GND  
18.RX#  
17.RX  
16.GND  
  
15.V33  
14.V33  
13.V33  
12.GND  
11.GND  
10.GND  
9.V5  
8.V5  
7.V5  
6.GND  
5.Reserved  
4.GND  
3.V12  
2.V12  
1.V12



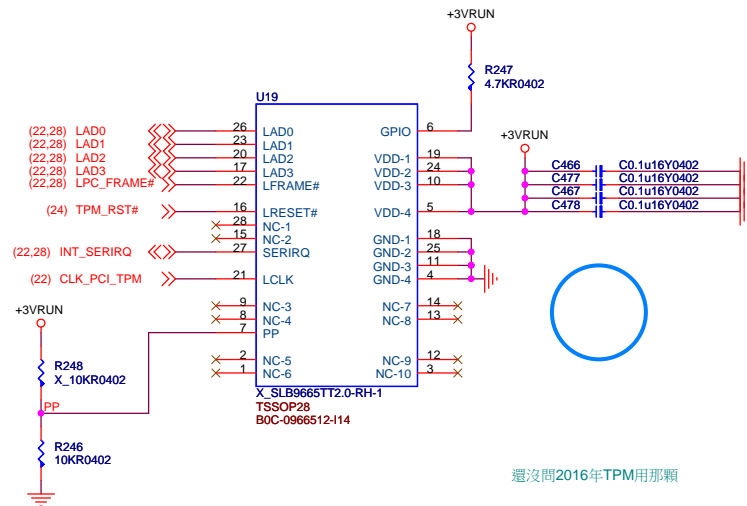


[illegible]

CNT 替換H=8.5mm



## TPM

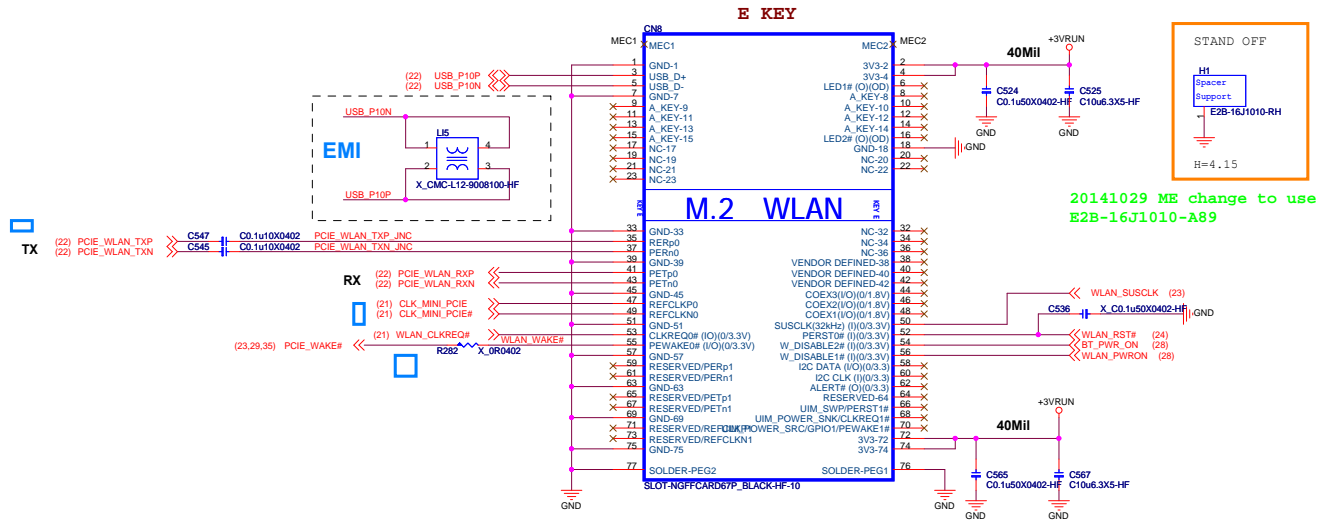


還沒問2016年TPM用那顆

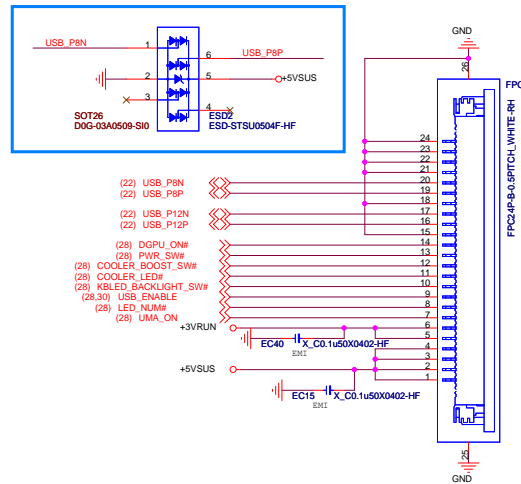
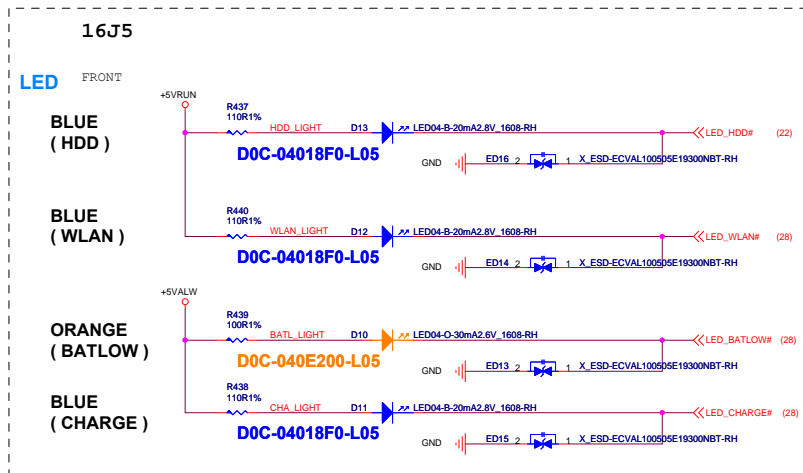


## WLAN

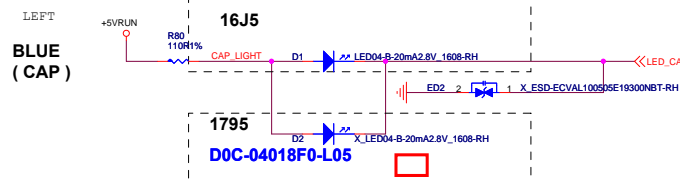
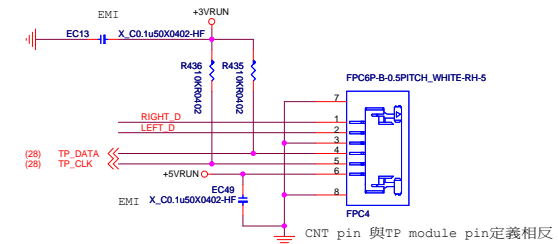
## WLAN/LED



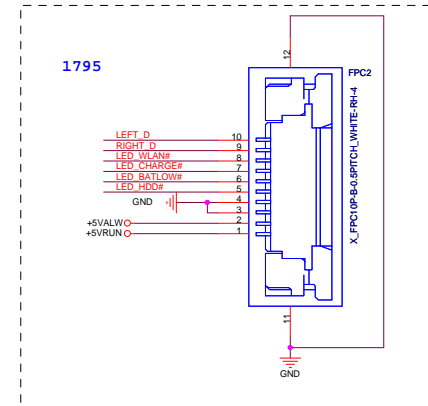
Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	Module Key	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (1 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKED#	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	N/C	Pin 64	N/C
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	N/C	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		



## Touch Pad



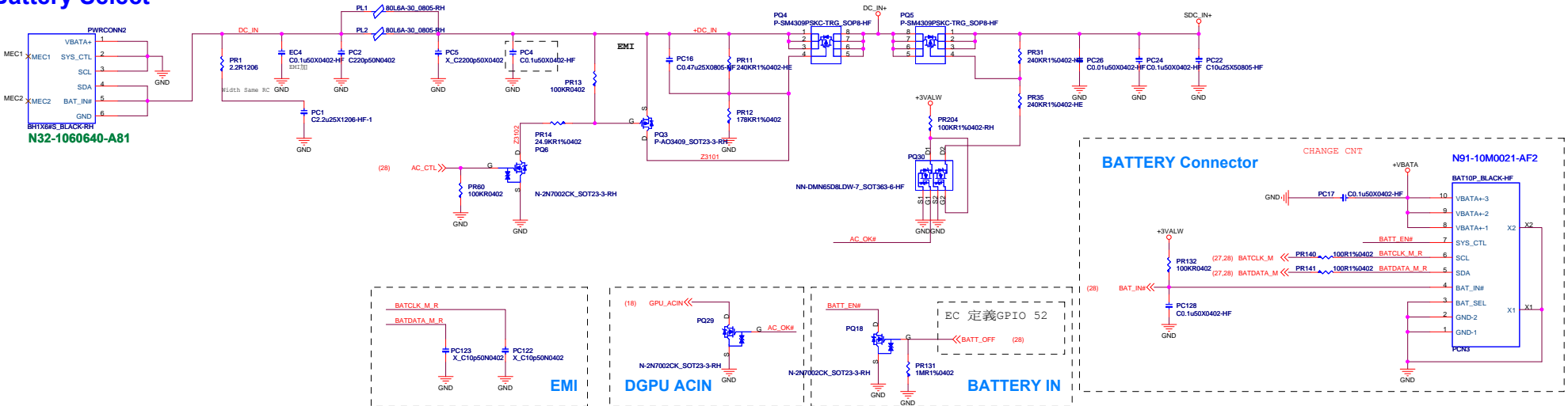
## 1795



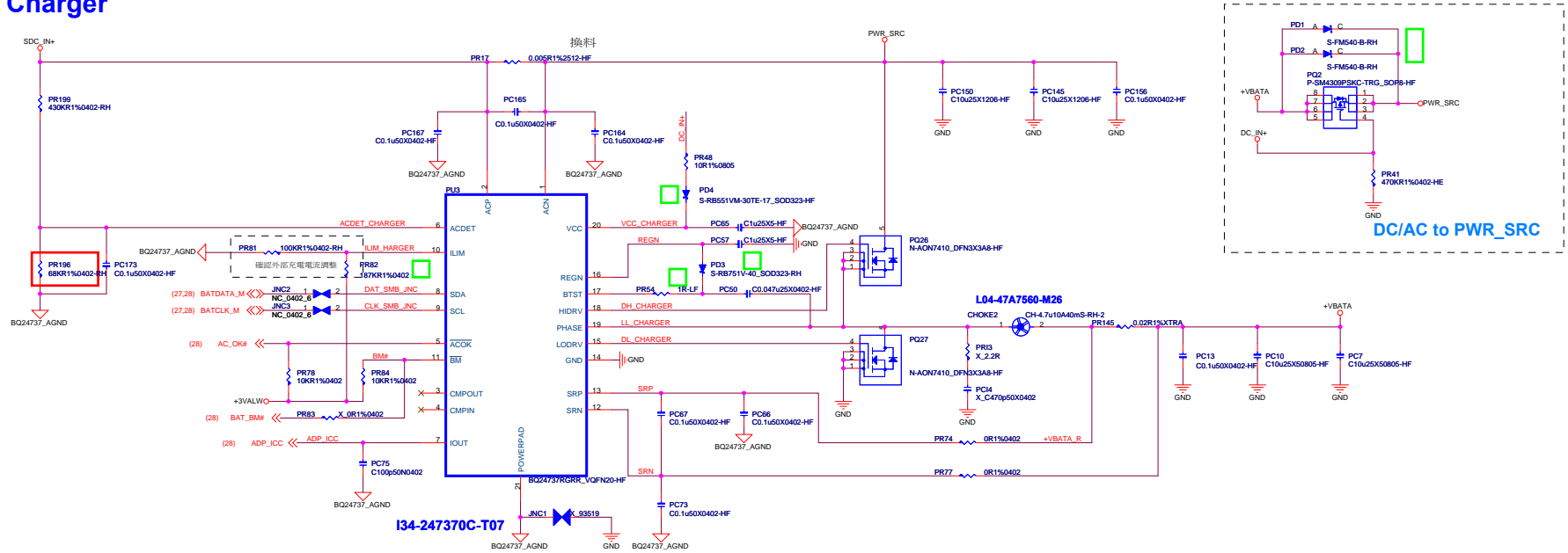


# Battery Select/Charger

## Battery Select

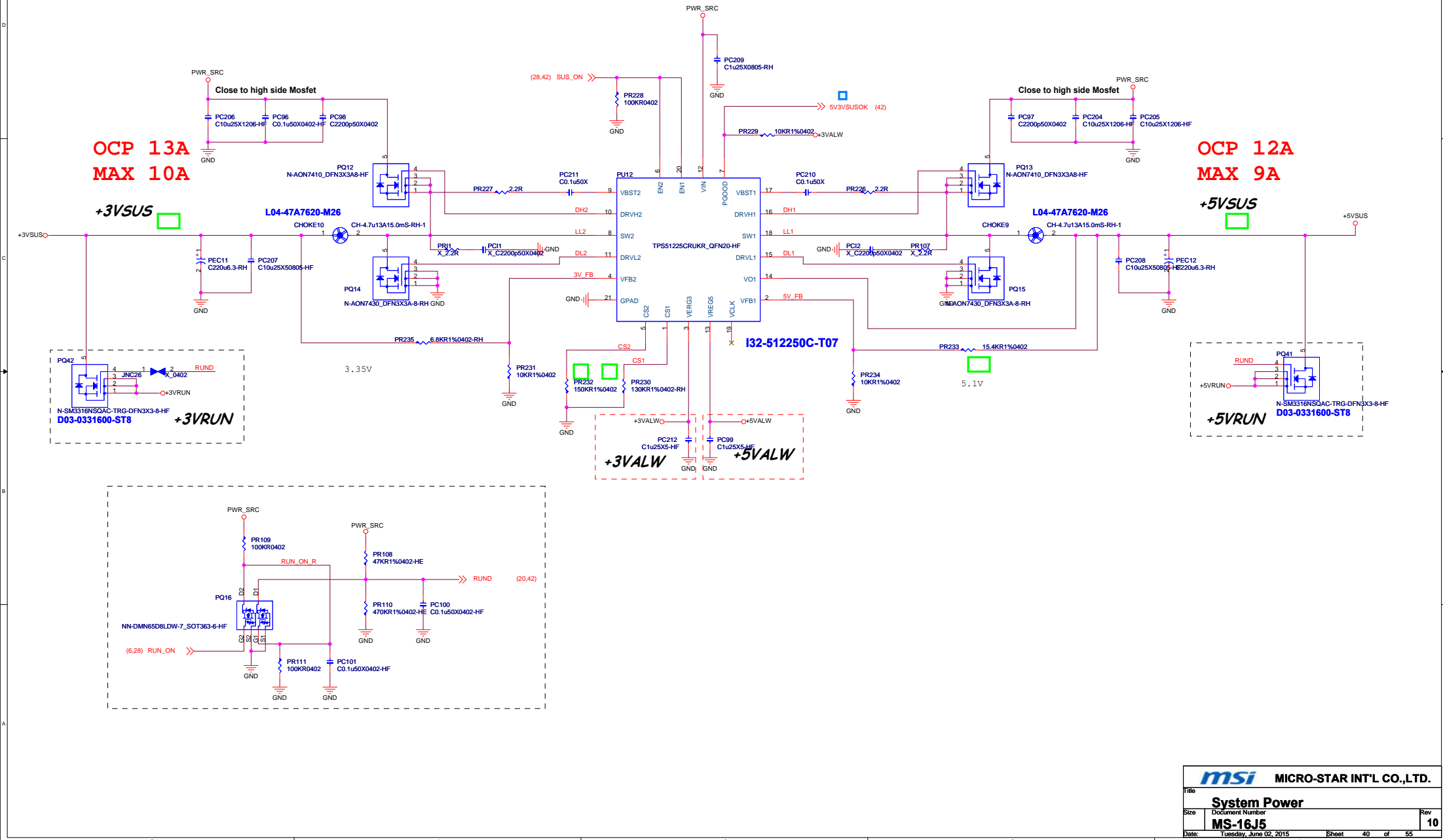


## Battery Charger





## System Power

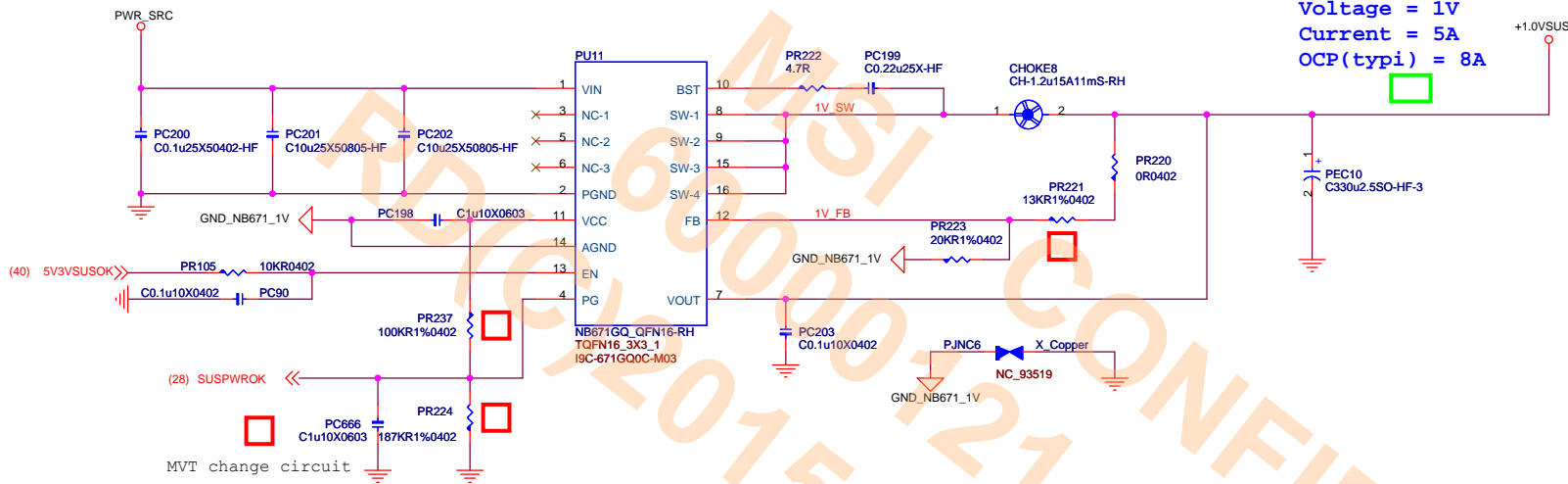




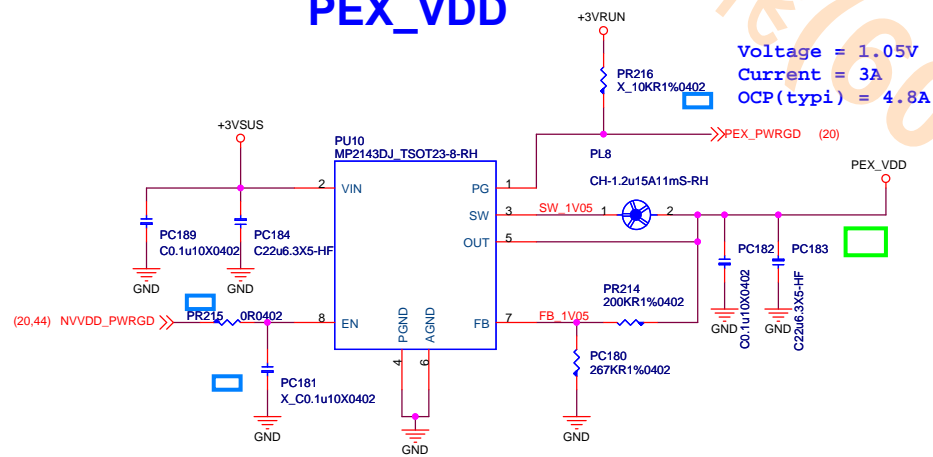




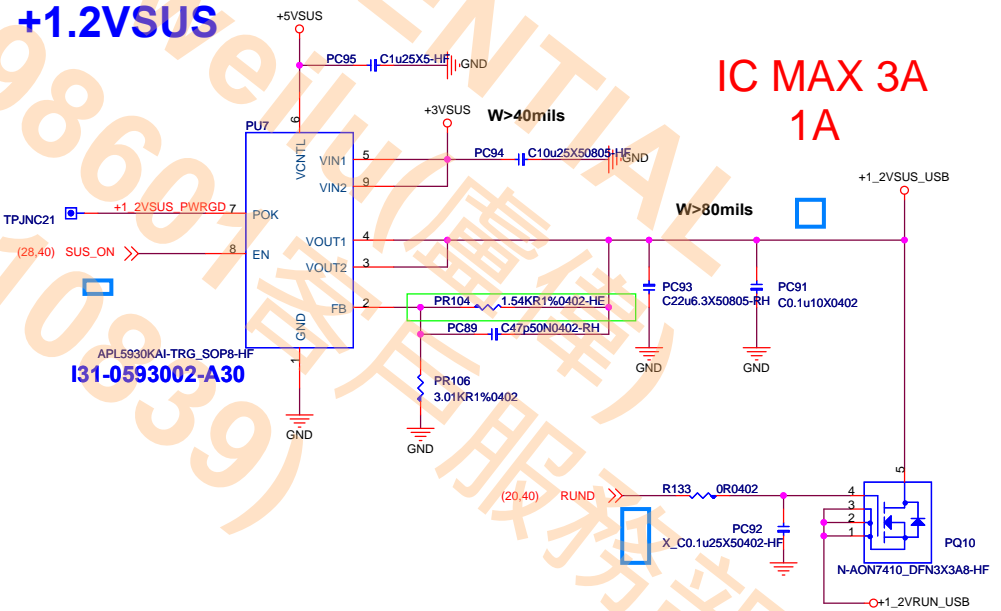
# +1VSUS



# PEX\_VDD



# +1.2VSUS

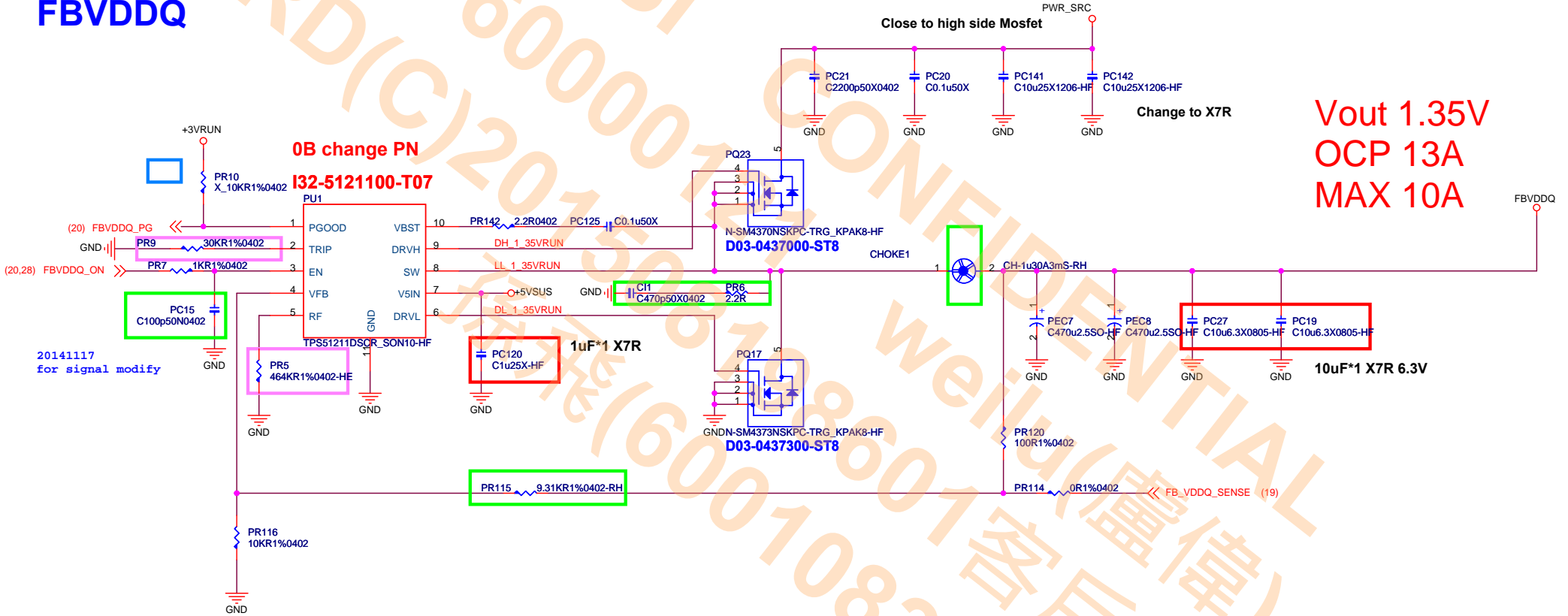




# DGPU POWER FBVDDQ

FBVDDQ

0B change PN  
I32-5121100-T07





# DGPU POWER / UP1642PQAG

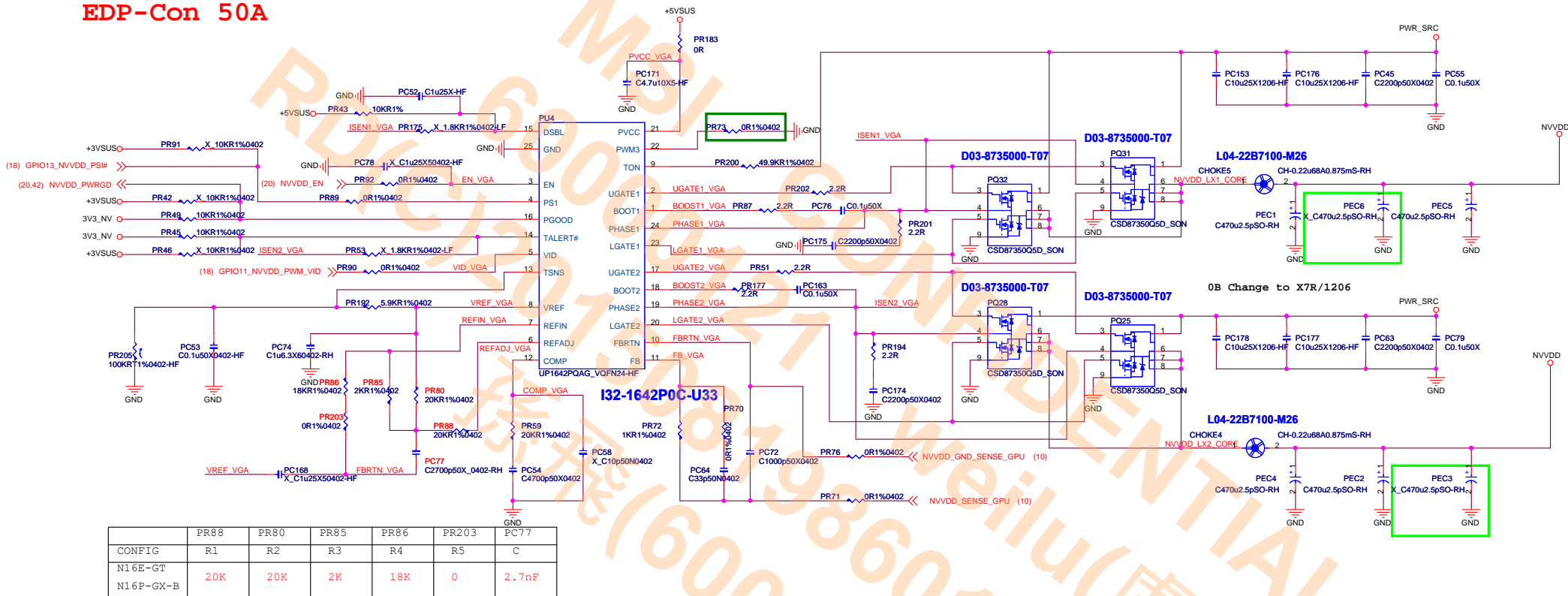
EDP-Peak 87A  
EDP-Con 50A

# DGPU POWER NVVDD

CONFIG A

VBoot:0.875V

Vmin:0.6V / Vmax:1.2V



20141029 power modify for GPU power setting

PR52,PR56: 39K ohm to 20K ohm

PR53: 1.5K ohm to 2K ohm

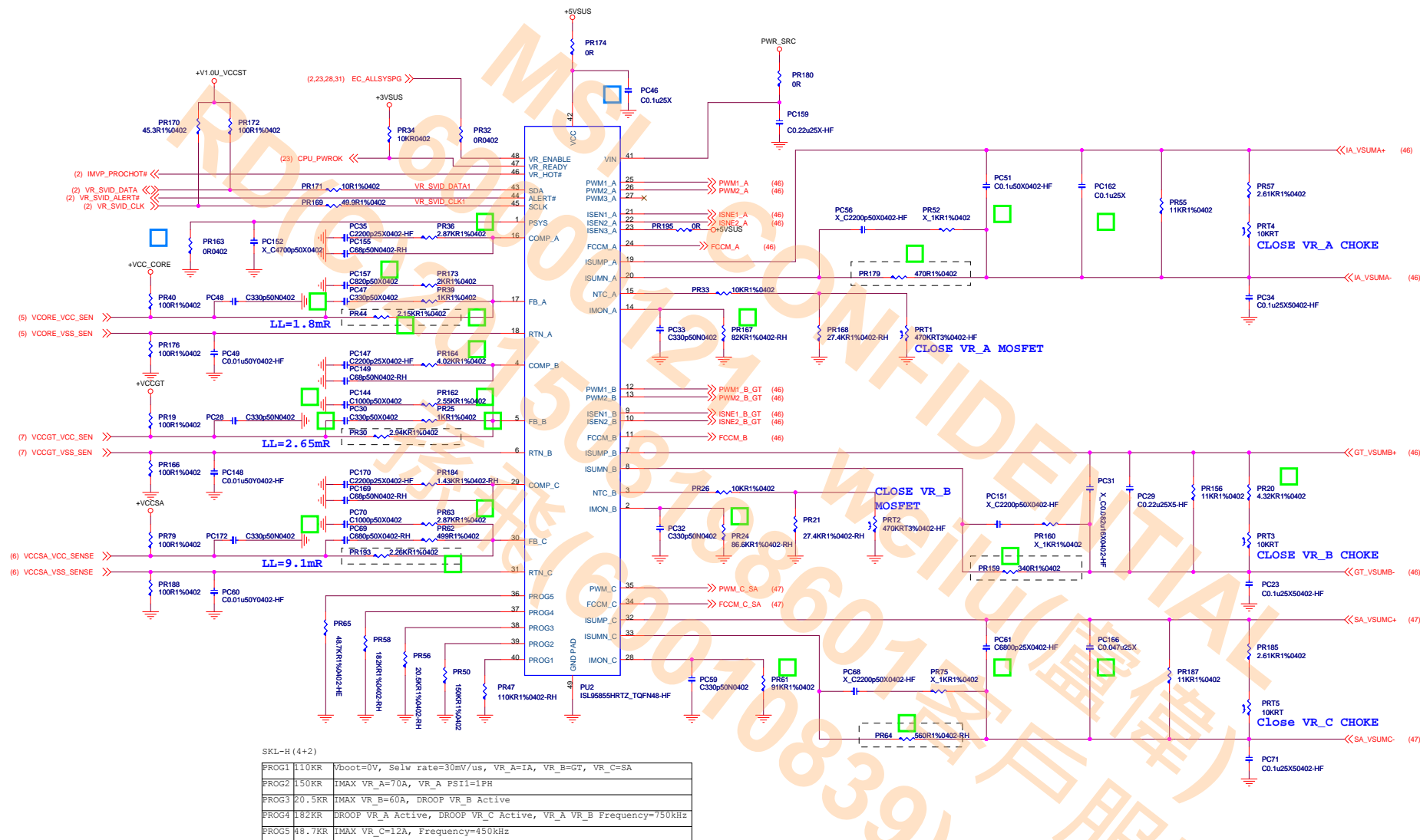
PR54: 30K ohm to 18K ohm

PR121: 1.5K ohm to 0 ohm

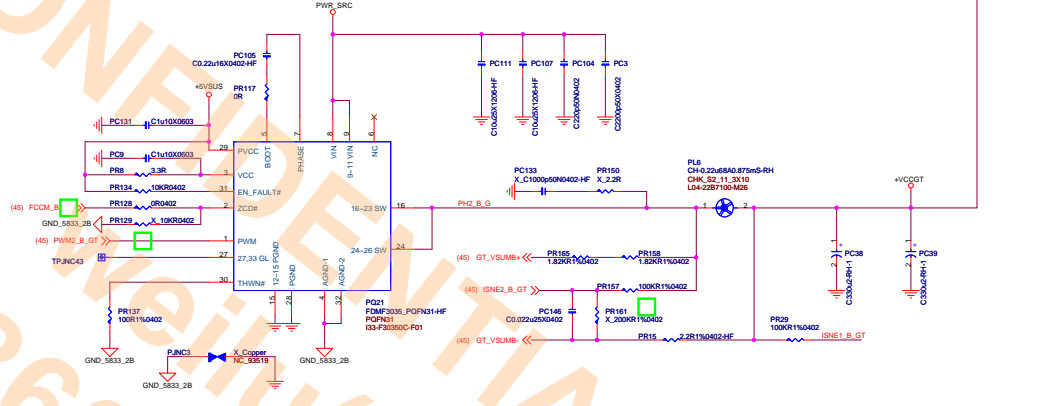
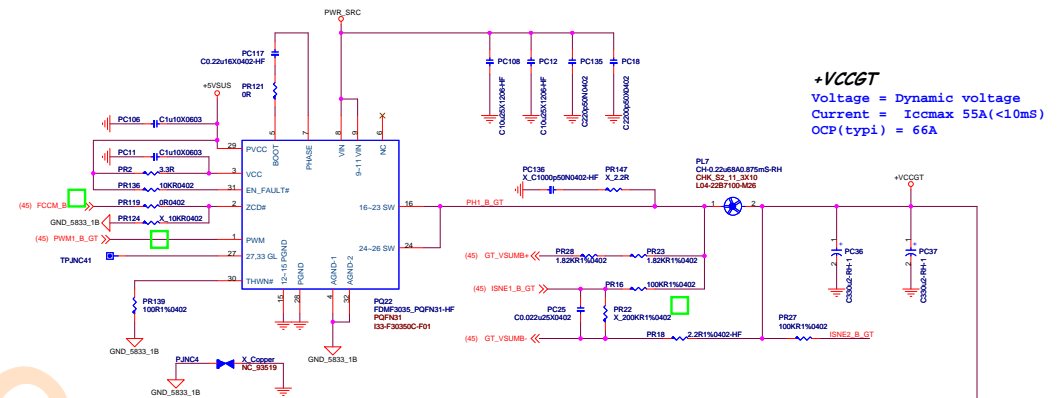
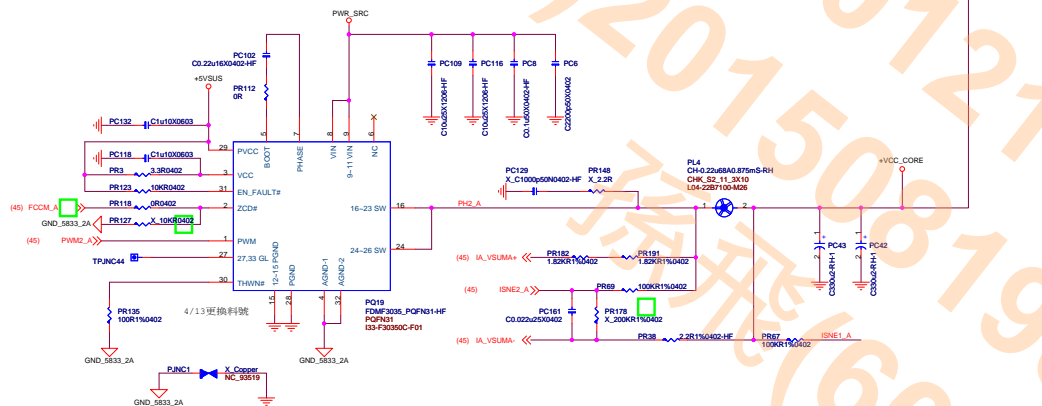
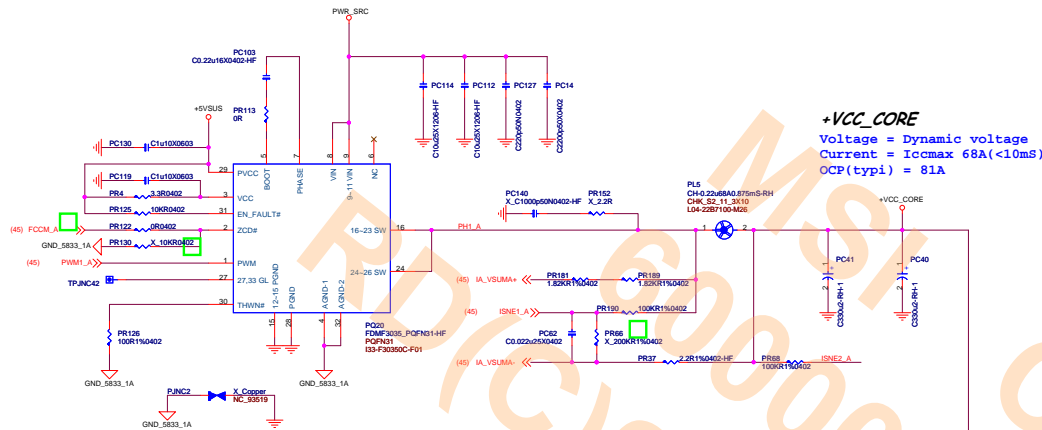
PC45: 1.5nF to 2.7nF



## Skylake H-line 42 45W ISL95855



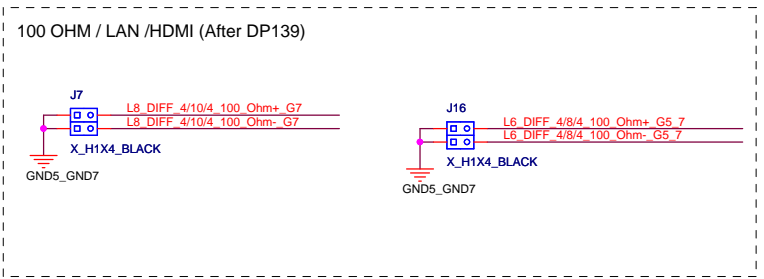
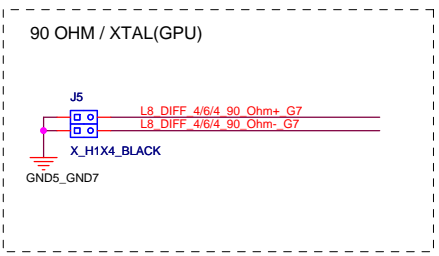
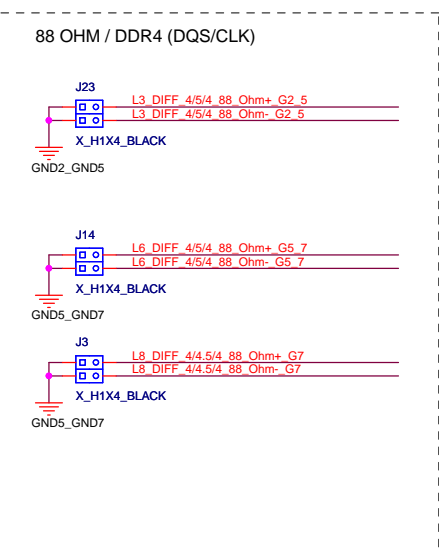
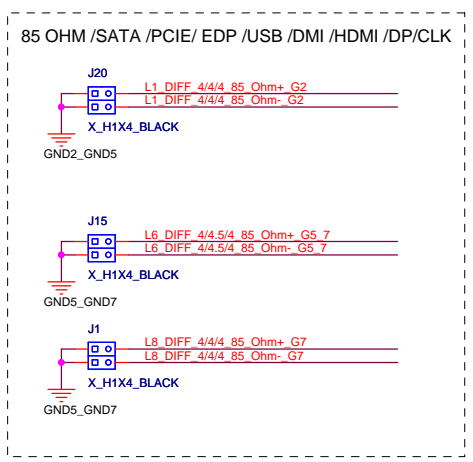
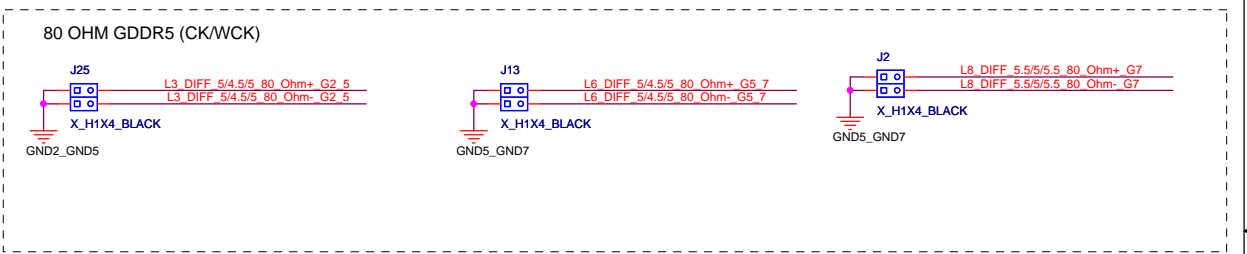
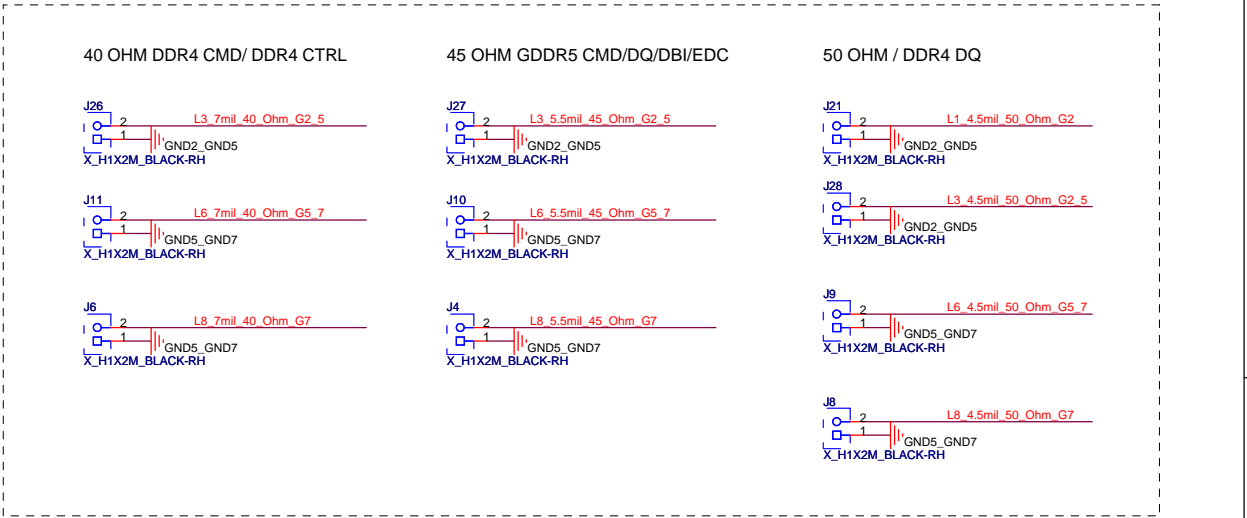
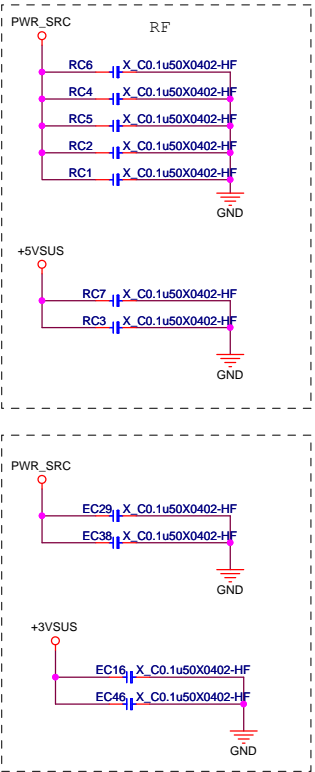
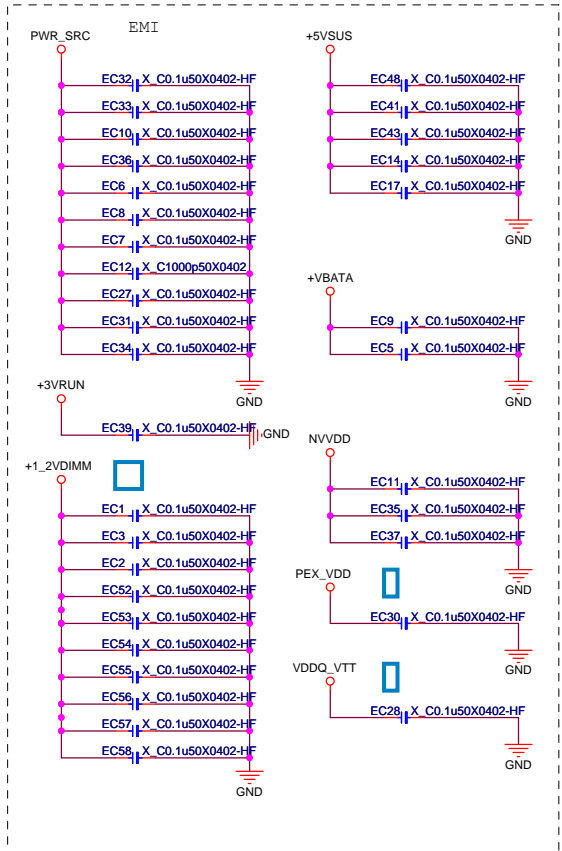






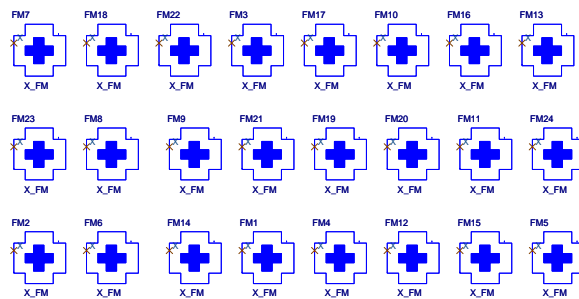
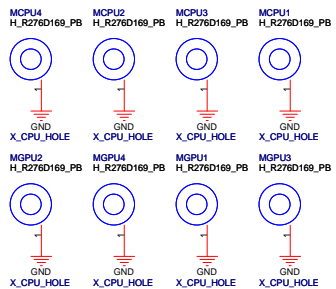




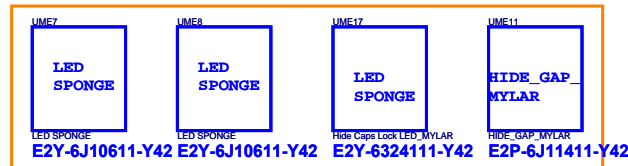




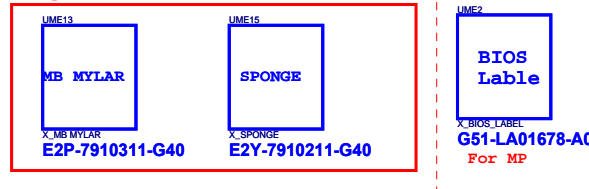
## CPU/GPU Holes



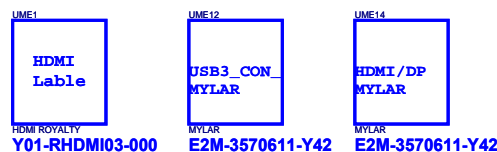
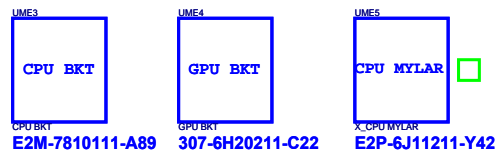
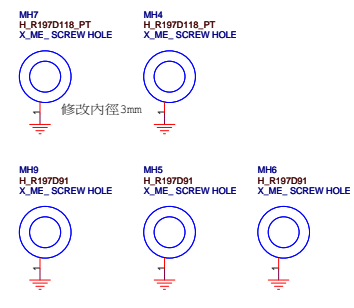
Only 16J5



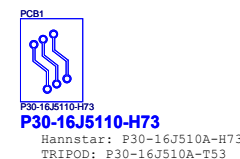
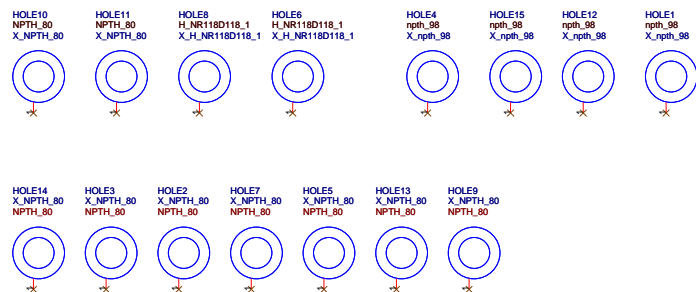
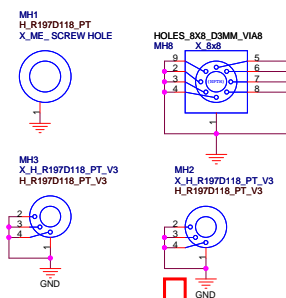
Only 1795



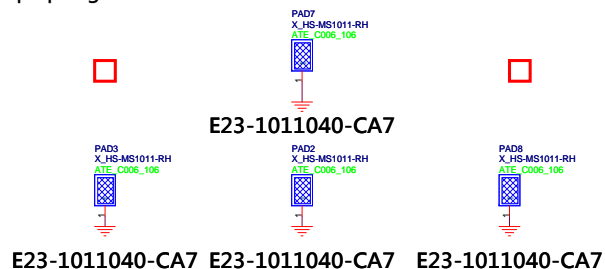
## OD 2.3



## 版邊 內3 / 外8



## Top Spring



## BOT Spring

